5.4 CHARACTERISTICS OF THE SPI BUS

The SPI bus consists of two serial data lines (MISO and MOSI), a clock line (SCK), and a Slave Select line ($\overline{SS}$).

5.4.1 Overview

During an SPI transfer, a byte is shifted out one data pin while a different byte is simultaneously shifted in through a second data pin. It can be viewed as two 8-bit shift registers connected together in a circular manner, where one shift register is located on the master side and the other on the slave side. Thus the data bytes in the master device and slave device are effectively exchanged. The MISO and MOSI data pins are used for transmitting and receiving serial data. When the SPI is configured as a master, MISO is the master data input line, and MOSI is the master data output line. When the SPI is configured as a slave device, these pins reverse roles.

Clock control logic allows a selection of clock polarity and a choice of two fundamentally different clocking protocols to accommodate most available synchronous serial peripheral devices. When the SPI is configured as a master, the control bits in the HCKR select the appropriate clock rate, as well as the desired clock polarity and phase format (see **Figure 5-6** on page 5-11).

The $\overline{SS}$ line allows individual selection of a slave SPI device; slave devices that are not selected do not interfere with SPI bus activity (i.e., they keep their MISO output pin in the high-impedance state). When the SHI is configured as an SPI master device, the $\overline{SS}$ line should be held high. If the $\overline{SS}$ line is driven low when the SHI is in SPI Master mode, a bus error will be generated (the HCSR HBER bit will be set).

5.5 CHARACTERISTICS OF THE I²C BUS

The I²C serial bus consists of two bi-directional lines, one for data signals (SDA) and one for clock signals (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

Note: Within the I²C bus specifications, a low-speed mode (2 kHz clock rate) and a high-speed mode (100 kHz clock rate) are defined. The SHI operates in the high-speed mode only.

5.5.1 Overview

The I²C bus protocol must conform to the following rules:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line when the clock line is high will be interpreted as control signals (see **Figure 5-7**).

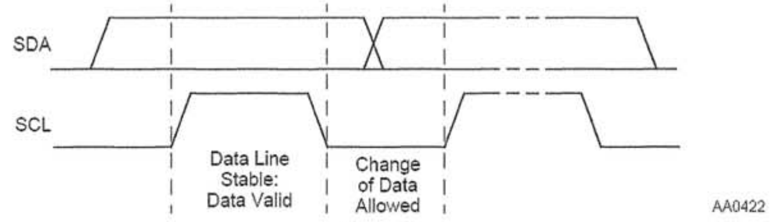

Figure 5-7 I²C Bit Transfer

Accordingly, the I²C bus protocol defines the following events:

- **Bus not busy**—Both data and clock lines remain high.
- **Start data transfer**—The Start event is defined as a change in the state of the data line, from high to low, while the clock is high (see **Figure 5-8**).

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- **Stop data transfer**—The Stop event is defined as a change in the state of the data line, from low to high, while the clock is high (see **Figure 5-8**).

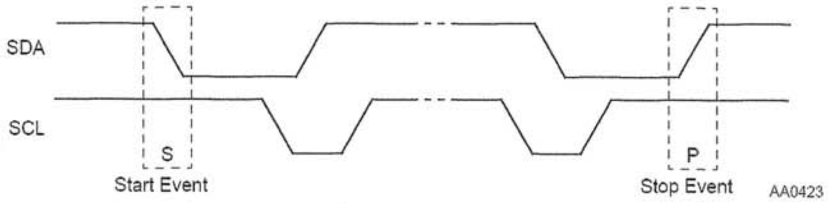

Figure 5-8 I^2C Start and Stop Events

- **Data valid**—The state of the data line represents valid data when, after a Start event, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each 8-bit word is followed by one acknowledge bit. This acknowledge bit is a high level put on the bus by the transmitter when the master device generates an extra acknowledge-related clock pulse. A slave receiver that is addressed is obliged to generate an acknowledge after the reception of each byte. Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge-related clock pulse (see **Figure 5-9**).

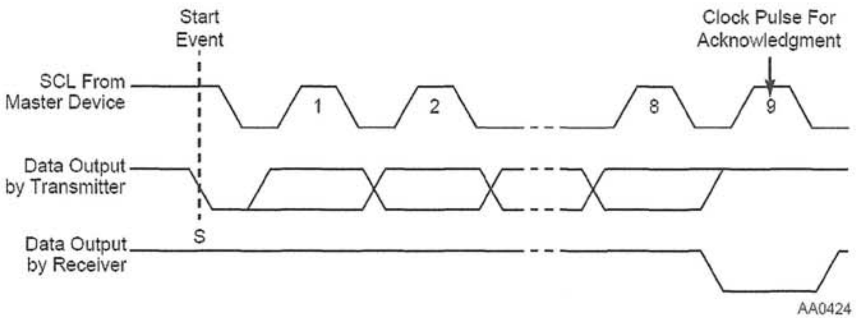

Figure 5-9 Acknowledgment on the I^2C Bus

By definition, a device that generates a signal is called a "transmitter," and the device that receives the signal is called a "receiver." The device that controls the signal is called the "master" and the devices that are controlled by the master are called "slaves". A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave device. In this case the transmitter must leave the data line high to enable the master generation of the Stop event. Handshaking may also be accomplished by use of the clock synchronizing mechanism. Slave devices can hold the SCL line low, after receiving and acknowledging a byte, to force the master into a wait state until the slave device is ready for the next byte transfer. The SHI supports this feature when operating as a master device and will wait until the slave device releases the SCL line before proceeding with the data transfer.

5.5.2 I ^{2}C Data Transfer Formats

I^2C bus data transfers follow the following format: after the Start event, a slave device address is sent. This address is 7 bits wide, the eighth bit is a data direction bit ($R/\overline{W}$); '0' indicates a transmission (write), and '1' indicates a request for data (read). A data transfer is always terminated by a Stop event generated by the master device. However, if the master device still wishes to communicate on the bus, it can generate another Start event, and address another slave device without first generating a Stop event (this feature is not supported by the SHI when operating as an I^2C master device). This method is also used to provide indivisible data transfers. Various combinations of read/write formats are illustrated in **Figure 5-10** and **Figure 5-11**.

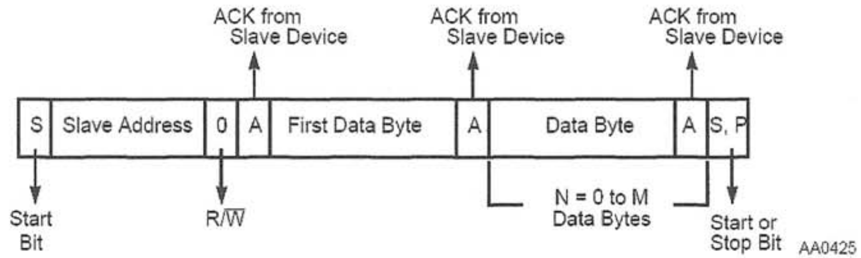

Figure 5-10 I^2C Bus Protocol For Host Write Cycle

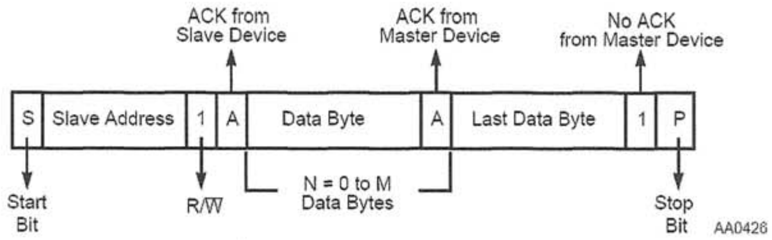

Figure 5-11 I^2C Bus Protocol For Host Read Cycle

Note: The first data byte in a write-bus cycle can be used as a user-predefined control byte (e.g., to determine the location to which the forthcoming data bytes should be transferred).

5.6 SHI PROGRAMMING CONSIDERATIONS

The SHI implements both SPI and I^2C bus protocols and can be programmed to operate as a slave device or a single-master device. Once the operating mode is selected, the SHI may communicate with an external device by receiving and/or transmitting data. Before changing the SHI operational mode, an SHI individual reset should be generated by clearing the HEN bit. The following paragraphs describe programming considerations for each operational mode.

5.6.1 SPI Slave Mode

The SPI Slave mode is entered by enabling the SHI (HEN = 1), selecting the SPI mode (HI^2C = 0), and selecting the Slave mode of operation (HMST = 0). The programmer should verify that the CPHA and CPOL bits (in the HCKR) correspond to the external host clock phase and polarity. Other HCKR bits are ignored. When configured in the SPI Slave mode, the SHI external pins operate as follows:

- SCK/SCL is the SCK serial clock input.
- MISO/SDA is the MISO serial data output.
- MOSI/HA0 is the MOSI serial data input.
- $\overline{SS}$/HA2 is the $\overline{SS}$ Slave Select input.
- $\overline{HREQ}$ is the Host Request output.

In the SPI Slave mode, a receive, transmit, or full-duplex data transfer may be performed. Actually, the interface simultaneously performs both data receive and transmit. The status bits of both receive and transmit paths are active, however, the programmer may disable undesired interrupts and ignore non-relevant status bits. It is recommended that an SHI individual reset (HEN cleared) be generated before beginning data reception in order to reset the HRX FIFO to its initial (empty) state (e.g., when switching from transmit to receive data).

If a write to HTX occurs, its contents are transferred to IOSR between data word transfers. The IOSR data is shifted out (via MISO) and received data is shifted in (via MOSI). The DSP may write HTX if the HTDE status bit is set. If no writes to HTX occurred, the contents of HTX are not transferred to IOSR, so the data that is shifted out when receiving is the same as the data present in the IOSR shift register at the time. The HRX FIFO contains valid receive data, which may be read by the DSP, if the HRNE status bit is set.

The $\overline{HREQ}$ output pin, if enabled for receive (HRQE1–HRQE0 = 01), is asserted when the IOSR is ready for receive and the HRX FIFO is not full; this operation guarantees that the next received data word will be stored in the FIFO. The $\overline{HREQ}$ output pin, if enabled for transmit (HRQE1–HRQE0 = 10), is asserted when the IOSR is loaded from HTX with a new data word to transfer. If $\overline{HREQ}$ is enabled for both transmit and receive (HRQE1–HRQE0 = 11), it is asserted when the receive and transmit conditions are true simultaneously. $\overline{HREQ}$ is deasserted at the first clock pulse of the next data word transfer. The $\overline{HREQ}$ line may be used to interrupt the external master device. Connecting the $\overline{HREQ}$ line between two SHI-equipped DSPs, one operating as an SPI master device and the other as an SPI slave device, enables full hardware handshaking if operating with CPHA = 1.

The $\overline{SS}$ line should be kept asserted during a data word transfer. If the $\overline{SS}$ line is deasserted before the end of the data word transfer, the transfer is aborted and the received data word is lost.

5.6.2 SPI Master Mode

The SPI Master mode is initiated by enabling the SHI (HEN = 1), selecting the SPI mode (HI^2C = 0), and selecting the Master mode of operation (HMST = 1). Before enabling the SHI as an SPI master device, the programmer should program the proper clock rate, phase, and polarity in HCKR. When configured in the SPI Master mode, the SHI external pins operate as follows:

- SCK/SCL is the SCK serial clock output.

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- MISO/SDA is the MISO serial data input.
- MOSI/HA0 is the MOSI serial data output.
- $\overline{SS}$/HA2 is the SS input. It should be kept deasserted (high) for proper operation.
- $\overline{HREQ}$ is the Host Request input.

The external slave device can be selected either by using external logic or by activating a GPIO pin connected to its $\overline{SS}$ pin. However, the $\overline{SS}$ input pin of the SPI master device should be held deasserted (high) for proper operation. If the SPI master device $\overline{SS}$ pin is asserted, the Host Bus Error status bit (HBER) is set. If the HBIE bit is also set, the SHI issues a request to the DSP interrupt controller to service the SHI Bus Error interrupt.

In the SPI Master mode the DSP must write to HTX to receive, transmit, or perform a full-duplex data transfer. Actually, the interface performs simultaneous data receive and transmit. The status bits of both receive and transmit paths are active; however, the programmer may disable undesired interrupts and ignore non-relevant status bits. In a data transfer, the HTX is transferred to IOSR, clock pulses are generated, the IOSR data is shifted out (via MOSI) and received data is shifted in (via MISO). The DSP programmer may write HTX (if the HTDE status bit is set) to initiate the transfer of the next word. The HRX FIFO contains valid receive data, which may be read by the DSP, if the HRNE status bit is set.

Note: Motorola recommends that an SHI individual reset (HEN cleared) be generated before beginning data reception in order to reset the receive FIFO to its initial (empty) state, such as when switching from transmit to receive data.

The $\overline{HREQ}$ input pin is ignored by the SPI master device if the HRQE[1:0] bits are cleared, and considered if any of them is set. When asserted by the slave device, $\overline{HREQ}$ indicates that the external slave device is ready for the next data transfer. As a result, the SPI master sends clock pulses for the full data word transfer. $\overline{HREQ}$ is deasserted by the external slave device at the first clock pulse of the new data transfer. When deasserted, $\overline{HREQ}$ will prevent the clock generation of the next data word transfer until it is asserted again. Connecting the $\overline{HREQ}$ line between two SHI-equipped DSPs, one operating as an SPI master device and the other as an SPI slave device, enables full hardware handshaking if CPHA = 1. For CPHA = 0, $\overline{HREQ}$ should be disabled by clearing HRQE[1:0].

5.6.3 I ^{2}C Slave Mode

The I^{2}C Slave mode is entered by enabling the SHI (HEN = 1), selecting the I^{2}C mode (HI^{2}C = 1), and selecting the Slave mode of operation (HMST = 0). In this operational mode the contents of HCKR are ignored. When configured in the I^{2}C Slave mode, the SHI external pins operate as follows:

- SCK/SCL is the SCL serial clock input.
- MISO/SDA is the SDA open drain serial data line.
- MOSI/HA0 is the HA0 slave device address input.
- $\overline{SS}$/HA2 is the HA2 slave device address input.
- $\overline{HREQ}$ is the Host Request output.

When the SHI is enabled and configured in the I^{2}C Slave mode, the SHI controller inspects the SDA and SCL lines to detect a Start event. Upon detection of the Start event, the SHI receives the slave device address byte and enables the slave device address recognition unit. If the slave device address byte was not identified as its personal address, the SHI controller will fail to acknowledge this byte by not driving low the SDA line at the ninth clock pulse (ACK = 1). However, it continues to poll the SDA and SCL lines to detect a new Start event. If the personal slave device address was correctly identified, the slave device address byte is acknowledged (ACK = 0 is sent) and a receive/transmit session is initiated according to the eighth bit of the received slave device address byte (i.e., the R/$\overline{W}$ bit).

5.6.3.1 Receive Data in I^{2}C Slave Mode

A receive session is initiated when the personal slave device address has been correctly identified and the R/$\overline{W}$ bit of the received slave device address byte has been cleared. Following a receive initiation, data in the SDA line is shifted into IOSR MSB first. Following each received byte, an acknowledge (ACK = 0) is sent at the ninth clock pulse via the SDA line. Data is acknowledged bytewise, as required by the I^{2}C bus protocol, and is transferred to the HRX FIFO when the complete word (according to HM0–HM1) is filled into IOSR. It is the responsibility of the programmer to select the correct number of bytes in an I^{2}C frame so that they fit in a complete number of words. For this purpose, the slave device address byte does not count as part of the data, and therefore, it is treated separately.

In a receive session, only the receive path is enabled and HTX to IOSR transfers are inhibited. The HRX FIFO contains valid data, which may be read by the DSP if the HRNE status bit is set. When the HRX FIFO is full and IOSR is filled, an overrun error occurs and the HROE status bit is set. In this case, the last received byte will not be acknowledged (ACK = 1 is sent) and the word in the IOSR will not be transferred to the HRX FIFO. This may inform the external I^{2}C master device of the occurrence of an overrun error on the slave side. Consequently the I^{2}C master device may terminate this session by generating a Stop event.

The $\overline{HREQ}$ output pin, if enabled for receive (HRQE1–HRQE0 = 01), is asserted when the IOSR is ready to receive and the HRX FIFO is not full; this operation guarantees that the next received data word will be stored in the FIFO. $\overline{HREQ}$ is deasserted at the first clock pulse of the next received word. The $\overline{HREQ}$ line may be used to interrupt the external I^{2}C master device. Connecting the $\overline{HREQ}$ line between two SHI-equipped DSPs, one operating as an I^{2}C master device and the other as an I^{2}C slave device, enables full hardware handshaking.

5.6.3.2 Transmit Data In I^{2}C Slave Mode

A transmit session is initiated when the personal slave device address has been correctly identified and the R/$\overline{W}$ bit of the received slave device address byte has been set. Following a transmit initiation, the IOSR is loaded from HTX (assuming the latter was not empty) and its contents are shifted out, MSB first, on the SDA line. Following each transmitted byte, the SHI controller samples the SDA line at the ninth clock pulse, and inspects the ACK status. If the transmitted byte was acknowledged (ACK = 0), the SHI controller continues and transmits the next byte. However, if it was not acknowledged (ACK = 1), the transmit session is stopped and the SDA line is released. Consequently, the external master device may generate a Stop event in order to terminate the session.

HTX contents are transferred to IOSR when the complete word (according to HM0–HM1) has been shifted out. It is, therefore, the responsibility of the programmer to select the correct number of bytes in an I^{2}C frame so that they fit in a complete number of words. For this purpose, the slave device address byte does not count as part of the data, and therefore, it is treated separately.

In a transmit session, only the transmit path is enabled and the IOSR-to-HRX FIFO transfers are inhibited. When the HTX transfers its valid data word to IOSR, the HTDE status bit is set and the DSP may write a new data word to HTX. If both IOSR and HTX are empty, an underrun condition occurs, setting the HTUE status bit; if this occurs, the previous word will be retransmitted.

The $\overline{HREQ}$ output pin, if enabled for transmit (HRQE1–HRQE0 = 10), is asserted when HTX is transferred to IOSR for transmission. When asserted, $\overline{HREQ}$ indicates that the slave device is ready to transmit the next data word. $\overline{HREQ}$ is deasserted at the first clock pulse of the next transmitted data word. The $\overline{HREQ}$ line may be used to interrupt the external I^{2}C master device. Connecting the $\overline{HREQ}$ line between two SHI-equipped DSPs, one operating as an I^{2}C master device and the other as an I^{2}C slave device, enables full hardware handshaking.

5.6.4 I ^{2}C Master Mode

The I^{2}C Master mode is entered by enabling the SHI (HEN = 1), selecting the I^{2}C mode (HI^{2}C = 1) and selecting the master mode of operation (HMST = 1). Before enabling the SHI as an I^{2}C master, the programmer should program the appropriate clock rate in HCKR.

When configured in the I^{2}C Master mode, the SHI external pins operate as follows:

- SCK/SCL is the SCL serial clock output.
- MISO/SDA is the SDA open drain serial data line.
- MOSI/HA0 is the HA0 slave device address input.
- $\overline{SS}$/HA2 is the HA2 slave device address input.
- $\overline{HREQ}$ is the Host Request input.

In the I^{2}C Master mode, a data transfer session is always initiated by the DSP by writing to the HTX register when HIDLE is set. This condition ensures that the data byte written to HTX will be interpreted as being a slave address byte. This data byte must specify the slave device address to be selected and the requested data transfer direction.

Note: The slave address byte should be located in the high portion of the data word, whereas the middle and low portions are ignored. Only one byte (the slave address byte) will be shifted out, independent of the word length defined by the HM0–HM1 bits.

In order for the DSP to initiate a data transfer the following actions are to be performed:

- The DSP tests the HIDLE status bit.
- If the HIDLE status bit is set, the DSP writes the slave device address and the R/$\overline{W}$ bit to the most significant byte of HTX.
- The SHI generates a Start event.
- The SHI transmits one byte only, internally samples the R/$\overline{W}$ direction bit (last bit), and accordingly initiates a receive or transmit session.
- The SHI inspects the SDA level at the ninth clock pulse to determine the ACK value. If acknowledged (ACK = 0), it starts its receive or transmit session according to the sampled R/$\overline{W}$ value. If not acknowledged (ACK = 1), the

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HBER status bit in HCSR is set, which will cause an SHI Bus Error interrupt request if HBIE is set, and a Stop event will be generated.

The $\overline{HREQ}$ input pin is ignored by the I^{2}C master device if HRQE1 and HRQE0 are cleared, and considered if either of them is set. When asserted, $\overline{HREQ}$ indicates that the external slave device is ready for the next data transfer. As a result, the I^{2}C master device sends clock pulses for the full data word transfer. $\overline{HREQ}$ is deasserted by the external slave device at the first clock pulse of the next data transfer. When deasserted, $\overline{HREQ}$ will prevent the clock generation of the next data word transfer until it is asserted again. Connecting the $\overline{HREQ}$ line between two SHI-equipped DSPs, one operating as an I^{2}C master device and the other as an I^{2}C slave device, enables full hardware handshaking.

5.6.4.1 Receive Data in I^{2}C Master Mode

A receive session is initiated if the R/$\overline{W}$ direction bit of the transmitted slave device address byte is set. Following a receive initiation, data in SDA line is shifted into IOSR MSB first. Following each received byte, an acknowledge (ACK = 0) is sent at the ninth clock pulse via the SDA line if the HIDLE control bit is cleared. Data is acknowledged bytewise, as required by the I^{2}C bus protocol, and is transferred to the HRX FIFO when the complete word (according to HM0–HM1) is filled into IOSR. It is the responsibility of the programmer to select the correct number of bytes in an I^{2}C frame so that they fit in a complete number of words. For this purpose, the slave device address byte does not count as part of the data, and therefore, it is treated separately.

If the I^{2}C slave transmitter is acknowledged, it should transmit the next data byte. In order to terminate the receive session, the programmer should set the HIDLE bit at the last required data word. As a result, the last byte of the next received data word is not acknowledged, the slave transmitter releases the SDA line, and the SHI generates the Stop event and terminates the session.

In a receive session, only the receive path is enabled and the HTX-to-IOSR transfers are inhibited. If the HRNE status bit is set, the HRX FIFO contains valid data, which may be read by the DSP. When the HRX FIFO is full, the SHI suspends the serial clock just before acknowledge. In this case, the clock will be reactivated when the FIFO is read (the SHI gives an ACK = 0 and proceeds receiving) or when HIDLE is set (the SHI gives ACK = 1, generates the Stop event, and ends the receive session).

5.6.4.2 Transmit Data In I^{2}C Master Mode

A transmit session is initiated if the R/$\overline{W}$ direction bit of the transmitted slave device address byte is cleared. Following a transmit initiation, the IOSR is loaded from HTX (assuming HTX is not empty) and its contents are shifted out, MSB-first, on the SDA line. Following each transmitted byte, the SHI controller samples the SDA line at the ninth clock pulse, and inspects the ACK status. If the transmitted byte was acknowledged (ACK = 0), the SHI controller continues transmitting the next byte. However, if it was not acknowledged (ACK = 1), the HBER status bit is set to inform the DSP side that a bus error (or overrun, or any other exception in the slave device) has occurred. Consequently, the I^{2}C master device generates a Stop event and terminates the session.

HTX contents are transferred to the IOSR when the complete word (according to HM0–HM1) has been shifted out. It is, therefore, the responsibility of the programmer to select the right number of bytes in an I^{2}C frame so that they fit in a complete number of words. Remember that for this purpose, the slave device address byte does not count as part of the data.

In a transmit session, only the transmit path is enabled and the IOSR-to-HRX FIFO transfers are inhibited. When the HTX transfers its valid data word to the IOSR, the HTDE status bit is set and the DSP may write a new data word to HTX. If both IOSR and HTX are empty, the SHI will suspend the serial clock until new data is written into HTX (when the SHI proceeds with the transmit session) or HIDLE is set (the SHI reactivates the clock to generate the Stop event and terminate the transmit session).

5.6.5 SHI Operation During Stop

The SHI operation cannot continue when the DSP is in the Stop state, since no DSP clocks are active. While the DSP is in the Stop state, the SHI will remain in the individual reset state.

While in the individual reset state:

- SHI input pins are inhibited.
- Output and bidirectional pins are disabled (high impedance).
- The HCSR status bits and the transmit/receive paths are reset to the same state produced by hardware reset or software reset.
- The HCSR and HCKR control bits are not affected.

Note: Motorola recommends that the SHI be disabled before entering the Stop state.

LTC488/LTC489

Quad RS485 Line Receiver

FEATURES

- Low Power: I_{CC} = 7mA Typ
- Designed for RS485 or RS422 Applications
- Single 5V Supply
- –7V to 12V Bus Common Mode Range Permits ±7V Ground Difference Between Devices on the Bus
- 60mV Typical Input Hysteresis
- Receiver Maintains High Impedance in Three-State or with the Power Off
- 28ns Typical Receiver Propagation Delay
- Pin Compatible with the SN75173 (LTC488)
- Pin Compatible with the SN75175 (LTC489)

APPLICATIONS

- Low Power RS485/RS422 Receivers
- Level Translator

DESCRIPTION

The LTC®488 and LTC489 are low power differential bus/line receivers designed for multipoint data transmission standard RS485 applications with extended common mode range (12V to –7V). They also meet the requirements of RS422.

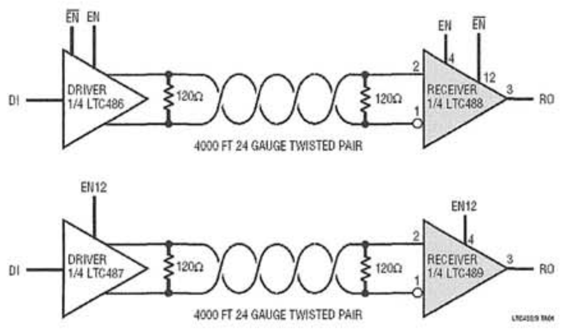
The CMOS design offers significant power savings over its bipolar counterpart without sacrificing ruggedness against overload or ESD damage.

The receiver features three-state outputs, with the receiver output maintaining high impedance over the entire common mode range.

The receiver has a fail-safe feature which guarantees a high output state when the inputs are left open.

Both AC and DC specifications are guaranteed 4.75V to 5.25V supply voltage range.

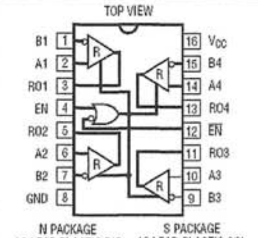
TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS (Note 1)

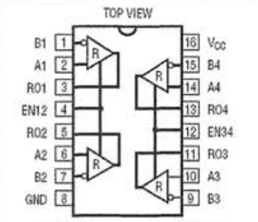
Supply Voltage (V_{CC}) 12V
Control Input Currents .... –25mA to 25mA
Control Input Voltages .... –0.5V to (V_{CC} + 0.5V)
Receiver Input Voltages .... ±14V
Receiver Output Voltages .... –0.5V to (V_{CC} + 0.5V)
Operating Temperature Range
LTC488C/LTC489C .... 0°C to 70°C
LTC488I/LTC489I .... –40°C to 85°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE 16-LEAD PLASTIC DIP; S PACKAGE 16-LEAD PLASTIC SOL
T_{JMAX} = 150°C, θ_{JA} = 70°C/W (N PKG)
T_{JMAX} = 150°C, θ_{JA} = 90°C/W (S PKG)

ORDER PART NUMBER
LTC488CN
LTC488CSW
LTC488IN
LTC488ISW



N PACKAGE 16-LEAD PLASTIC DIP; S PACKAGE 16-LEAD PLASTIC SOL
T_{JMAX} = 150°C, θ_{JA} = 70°C/W (N PKG)
T_{JMAX} = 150°C, θ_{JA} = 90°C/W (S PKG)

ORDER PART NUMBER
LTC489CN
LTC489CSW
LTC489IN
LTC489ISW

Consult factory for Military grade parts.

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V (Notes 2, 3), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{INH}	Input High Voltage	EN, $\overline{EN}$, EN12, EN34	●	2.0			V
V_{INL}	Input Low Voltage	EN, $\overline{EN}$, EN12, EN34	●			0.8	V
I_{IN1}	Input Current	EN, $\overline{EN}$, EN12, EN34	●			±2	μA
I_{IN2}	Input Current (A, B)	V_{CC} = 0V or 5.25V, V_{IN} = 12V V_{CC} = 0V or 5.25V, V_{IN} = –7V	● ●			1.0 –0.8	mA mA
V_{TH}	Differential Input Threshold Voltage for Receiver	–7V ≤ V_{CM} ≤ 12V	●	–0.2		0.2	V
ΔV_{TH}	Receiver Input Hysteresis	V_{CM} = 0V			60		mV
V_{OH}	Receiver Output High Voltage	I_O = –4mA, V_{ID} = 0.2V	●	3.5			V
V_{OL}	Receiver Output Low Voltage	I_O = 4mA, V_{ID} = –0.2V	●			0.4	V
I_{OZR}	Three-State Output Current at Receiver	V_{CC} = Max 0.4V ≤ V_O ≤ 2.4V	●			±1	μA
I_{CC}	Supply Current	No Load, Digital Pins = GND or V_{CC}	●		7	10	mA
R_{IN}	Receiver Input Resistance	–7V ≤ V_{CM} ≤ 12V, V_{CC} = 0V	●	12			kΩ
I_{OSR}	Receiver Short-Circuit Current	0V ≤ V_O ≤ V_{CC}	●	7		85	mA
t_{PLH}	Receiver Input to Output	C_L = 15pF (Figures 1, 3)	●	12	28	55	ns
t_{PHL}	Receiver Input to Output	C_L = 15pF (Figures 1, 3)	●	12	28	55	ns
t_{SKD}	$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew	C_L = 15pF (Figures 1, 3)			4		ns

Tournez la page S.V.P.

ANALOG DEVICES

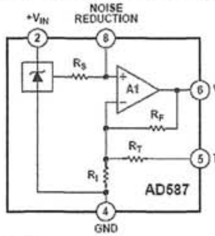
High Precision 10 V Reference

AD587

FEATURES

Laser trimmed to high accuracy
10.000 V ± 5 mV (U grade)
Trimmed temperature coefficient
5 ppm/°C maximum (U grade)
Noise-reduction capability
Low quiescent current: 4 mA maximum
Output trim capability
MIL-STD-883-compliant versions available

FUNCTIONAL BLOCK DIAGRAM



NOTE
PIN 1, PIN 3, AND PIN 7 ARE INTERNAL TEST POINTS. NO CONNECTIONS TO THESE POINTS.

Figure 1.

GENERAL DESCRIPTION

The AD587 represents a major advance in state-of-the-art monolithic voltage references. Using a proprietary ion-implanted buried Zener diode and laser wafer trimming of high stability thin-film resistors, the AD587 provides outstanding performance at low cost.

The AD587 offers much higher performance than most other 10 V references. Because the AD587 uses an industry-standard pinout, many systems can be upgraded instantly with the AD587.

The buried Zener approach to reference design provides lower noise and drift than band gap voltage references. The AD587 offers a noise-reduction pin that can be used to further reduce the noise level generated by the buried Zener.

The AD587 is recommended for use as a reference for 8-bit, 10-bit, 12-bit, 14-bit, or 16-bit DACs that require an external precision reference. The device is also ideal for successive approximation or integrating ADCs with up to 14 bits of accuracy. In general, it offers better performance than standard on-chip references.

The AD587J and AD587K are specified for operation from 0°C to 70°C, and the AD587U is specified for operation from −55°C to +125°C. The AD587JQ and AD587UQ models are available in 8-lead CERDIP. Other models are available in an 8-lead SOIC package for surface-mount applications, or in an 8-lead PDIP.

PRODUCT HIGHLIGHTS

1. Laser trimming of both initial accuracy and temperature coefficients. This laser trimming results in very low errors over temperature without the use of external components. The AD587U guarantees ±14 mV maximum total error between −55°C and +125°C.
2. Optional fine trim connection. This connection is designed for applications requiring higher precision.
3. Instant upgrade of any system using an industry-standard pinout 10 V reference.
4. Very low output noise. AD587 output noise is typically 4 μV p-p. A noise-reduction pin is provided for additional noise filtering using an external capacitor.
5. MIL-STD-883-compliant versions available. Refer to the Analog Devices *Military/Aerospace Reference Manual* for detailed specifications.

APPLICATIONS INFORMATION

USING THE AD587 WITH CONVERTERS

The AD587 is an ideal reference for a variety of 8-bit, 12-bit, 14-bit, and 16-bit ADCs and DACs. Several examples follow.

10 V Reference with Multiplying CMOS DACs or ADCs

The AD587 is ideal for applications with 10-bit and 12-bit multiplying CMOS DACs. In the standard hookup, shown in Figure 18, the AD587 is paired with the AD7545 12-bit multiplying DAC and the AD711 high speed BiFET op amp. The amplifier DAC configuration produces a unipolar 0 V to −10 V output range. Bipolar output applications and other operating details can be found in the individual product data sheets.

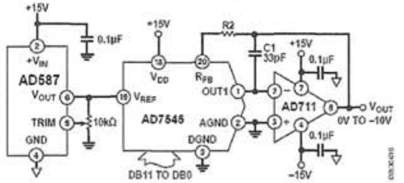


Figure 18. Low Power 12-Bit CMOS DAC Application

The AD587 can also be used as a precision reference for multiple DACs. Figure 19 shows the AD587, the AD7628 dual DAC, and the AD712 dual op amp hooked up for single-supply operation to produce 0 V to −10 V outputs. Because both DACs are on the same die and share a common reference and output op amps, the DAC outputs will exhibit similar gain temperature coefficients (TCs).

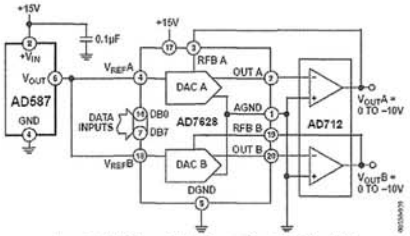


Figure 19. AD587 as a 10 V Reference for a CMOS Dual DAC

Precision Current Source

The design of the AD587 allows it to be easily configured as a current source. By choosing the control resistor (R_C) via the equation shown in Figure 20, the user can vary the load current from the quiescent current (2 mA typically) to approximately 10 mA.

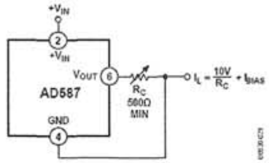


Figure 20. Precision Current Source

Precision High Current Supply

For higher currents, the AD587 can easily be connected to a power PNP or power Darlington PNP device. The circuits in Figure 21 and Figure 22 can deliver up to 4 A to the load. The 0.1 μF capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high frequency supply rejection results can be obtained by removing the capacitor.

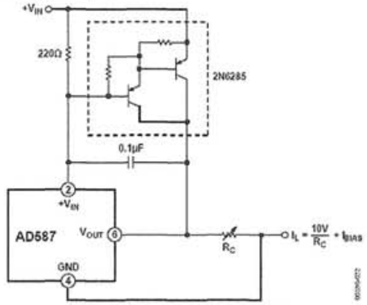


Figure 21. Precision High Current Source

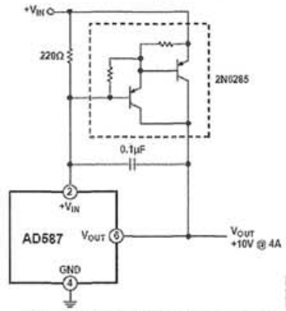


Figure 22. Precision High Current Voltage Source

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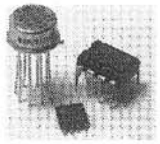


INA105

Precision Unity Gain DIFFERENTIAL AMPLIFIER

FEATURES

- CMR 86dB min OVER TEMPERATURE
- GAIN ERROR: 0.01% max
- NONLINEARITY: 0.001% max
- NO EXTERNAL ADJUSTMENTS REQUIRED
- EASY TO USE
- COMPLETE SOLUTION
- HIGHLY VERSATILE
- LOW COST
- PLASTIC DIP, TO-99 HERMETIC METAL, AND SO-8 SOIC PACKAGES

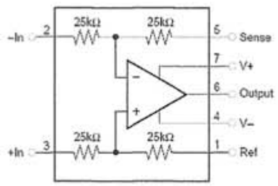
APPLICATIONS

- DIFFERENTIAL AMPLIFIER
- INSTRUMENTATION AMPLIFIER BUILDING BLOCK
- UNITY-GAIN INVERTING AMPLIFIER
- GAIN-OF-1/2 AMPLIFIER
- NONINVERTING GAIN-OF-2 AMPLIFIER
- AVERAGE VALUE AMPLIFIER
- ABSOLUTE VALUE AMPLIFIER
- SUMMING AMPLIFIER
- SYNCHRONOUS DEMODULATOR
- CURRENT RECEIVER WITH COMPLIANCE TO RAILS
- 4mA TO 20mA TRANSMITTER
- VOLTAGE-CONTROLLED CURRENT SOURCE
- ALL-PASS FILTERS

DESCRIPTION

The INA105 is a monolithic Gain = 1 differential amplifier consisting of a precision op amp and on-chip metal film resistors. The resistors are laser trimmed for accurate gain and high common-mode rejection. Excellent TCR tracking of the resistors maintains gain accuracy and common-mode rejection over temperature.

The differential amplifier is the foundation of many commonly used circuits. The INA105 provides this precision circuit function without using an expensive precision resistor network. The INA105 is available in 8-pin plastic DIP, SO-8 surface-mount and TO-99 metal packages.



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SPECIFICATIONS

ELECTRICAL

At +25°C, V_{CC} = ±15V, unless otherwise noted.

PARAMETER	CONDITIONS	INA105AM MIN	INA105AM TYP	INA105AM MAX	INA105BM MIN	INA105BM TYP	INA105BM MAX	INA105KP, KU MIN	INA105KP, KU TYP	INA105KP, KU MAX	UNITS
GAIN											
Initial(1)			1			*			*		V/V
Error			0.005	0.01		*	*		0.01	0.025	%
vs Temperature			1	5		*	*		*	*	ppm/°C
Nonlinearity(2)			0.0002	0.001		*	*		*	*	%
OUTPUT											
Rated Voltage	I_O = +20mA, –5mA	10	12		*	*		*	*		V
Rated Current	V_O = 10V	+20, –5			*			*			mA
Impedance			0.01			*			*		Ω
Current Limit	To Common		+40/–10			*			*		mA
Capacitive Load	Stable Operation		1000			*			*		pF
INPUT											
Impedance(3)	Differential		50			*			*		kΩ
	Common-Mode		50			*			*		kΩ
Voltage Range(4)	Differential	±10			*			*			V
	Common-Mode	±20			*			*			V
Common-Mode Rejection(5)	T_A = T_{MIN} to T_{MAX}	80	90		86	100		72	*		dB
OFFSET VOLTAGE	RTO(5), (7)										
Initial			50	250		*	*		*	500	µV
vs Temperature			5	20		5	10		*	*	µV/°C
vs Supply	$\pm V_S$ = 6V to 18V		1	25		*	15		*	*	µV/V
vs Time			20			*			*		µV/mo
OUTPUT NOISE VOLTAGE	RTO(5), (8)										
f_B = 0.01Hz to 10Hz			2.4			*			*		µVp-p
f_O = 10kHz			60			*			*		nV/√Hz
DYNAMIC RESPONSE											
Small Signal Bandwidth	–3dB		1			*			*		MHz
Full Power Bandwidth	V_O = 20Vp-p	30	50		*	*		*	*		kHz
Slew Rate		2	3		*	*		*	*		V/µs
Settling Time: 0.1%	V_O = 10V Step		4			*			*		µs
0.01%	V_O = 10V Step		5			*			*		µs
0.01%	V_{CM} = 10V Step, V_{DIFF} = 0V		1.5			*			*		µs
POWER SUPPLY											
Rated			±15			*			*		V
Voltage Range	Derated Performance	±5		±18	*		*	*		*	V
Quiescent Current	V_O = 0V		±1.5	±2		*	*		*	*	mA
TEMPERATURE RANGE											
Specification		–40		+85	*		*	*		*	°C
Operation		–55		+125	*		*	–40		+85	°C
Storage		–65		+150	*		*	–40		+125	°C

* Specification same as for INA105AM.

NOTES: (1) Connected as difference amplifier (see Figure 4). (2) Nonlinearity is the maximum peak deviation from the best-fit straight line as a percent of full-scale peak-to-peak output. (3) 25kΩ resistors are ratio matched but have ±20% absolute value. (4) Maximum input voltage without protection is 10V more than either ±15V supply (±25V). Limit I_{IN} to 1mA. (5) With zero source impedance (see "Maintaining CMR" section). (6) Referred to output in unity-gain difference configuration. Note that this circuit has a gain of 2 for the operational amplifier's offset voltage and noise voltage. (7) Includes effects of amplifier's input bias and offset currents. (8) Includes effects of amplifier's input current noise and thermal noise contribution of resistor network.

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Burr-Brown Products
from Texas Instruments

DAC7714

Quad, Serial Input, 12-Bit, Voltage Output DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW POWER: 250mW (max)
- UNIPOLAR OR BIPOLAR OPERATION
- SETTLING TIME: 10μs to 0.012%
- 12-BIT LINEARITY AND MONOTONICITY: –40°C to +85°C
- USER SELECTABLE RESET TO MID-SCALE OR ZERO-SCALE
- SECOND-SOURCE for DAC8420
- SMALL SO-16 PACKAGE

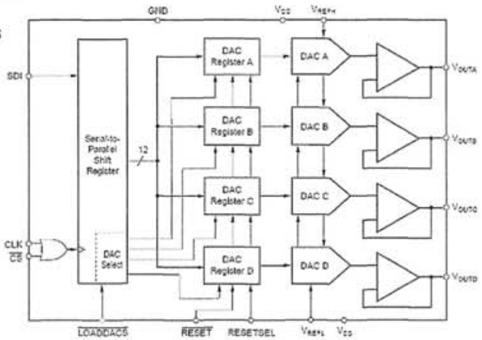
APPLICATIONS

- ATE PIN ELECTRONICS
- PROCESS CONTROL
- CLOSED-LOOP SERVO-CONTROL
- MOTOR CONTROL
- DATA ACQUISITION SYSTEMS

DESCRIPTION

The DAC7714 is a quad, serial input, 12-bit, voltage output Digital-to-Analog Converter (DAC) with guaranteed 12-bit monotonic performance over the –40°C to +85°C temperature range. An asynchronous reset clears all registers to either mid-scale (800_H) or zero-scale (000_H), selectable via the RESETSEL pin. The device can be powered from a single +15V supply or from dual +15V and –15V supplies.

Low power and small size makes the DAC7714 ideal for process control, data acquisition systems, and closed-loop servo-control. The device is available in a SO-16 package, and is guaranteed over the –40°C to +85°C temperature range.



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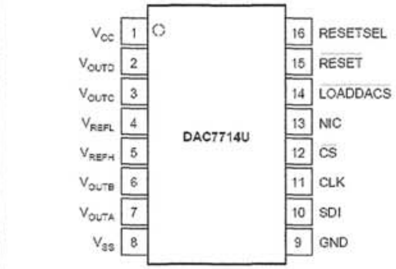
PIN CONFIGURATION—U Package



PIN DESCRIPTIONS—U Package

PIN	LABEL	DESCRIPTION
1	V_{CC}	Positive Analog Supply Voltage, +15V nominal.
2	V_{OUTD}	DAC D Voltage Output
3	V_{OUTC}	DAC C Voltage Output
4	V_{REFL}	Reference Input Voltage Low. Sets minimum output voltage for all DACs.
5	V_{REFH}	Reference Input Voltage High. Sets maximum output voltage for all DACs.
6	V_{OUTB}	DAC B Voltage Output
7	V_{OUTA}	DAC A Voltage Output
8	V_{SS}	Negative Analog Supply Voltage, 0V or –15V nominal.
9	GND	Ground
10	SDI	Serial Data Input
11	CLK	Serial Data Clock
12	$\overline{CS}$	Chip Select Input
13	NIC	Not Internally Connected
14	$\overline{LOADDACS}$	The selected DAC register becomes transparent when $\overline{LOADDACS}$ is LOW. It is in the latched state when $\overline{LOADDACS}$ is HIGH.
15	$\overline{RESET}$	Asynchronous Reset Input. Sets all DAC registers to either zero-scale (000_H) or mid-scale (800_H) when LOW. RESETSEL determines which code is active.
16	RESETSEL	When LOW, a LOW on $\overline{RESET}$ will cause all DAC registers to be set to code 000_H. When RESETSEL is HIGH, a LOW on $\overline{RESET}$ will set the registers to code 800_H.

SPECIFICATIONS (Dual Supply)

At $T_A = -40°C$ to $+85°C$, $V_{CC} = +15V$, $V_{SS} = -15V$, $V_{REFH} = +10V$, $V_{REFL} = -10V$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7714U			DAC7714UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Linearity Error				±2			±1	LSB(1)
Linearity Matching(2)				±2			±1	LSB
Differential Linearity Error				±1			±1	LSB
Monotonicity	T_{MIN} to T_{MAX}	12			*			Bits
Zero-Scale Error	Code = 000_H			±2			*	LSB
Zero-Scale Drift			1			*		ppm/°C
Zero-Scale Matching(2)				±2			±1	LSB
Full-Scale Error	Code = FFF_H			±2			*	LSB
Full-Scale Matching(2)				±2			±1	LSB
Power Supply Sensitivity	At Full Scale		10			*		ppm/V
ANALOG OUTPUT								
Voltage Output(3)		V_{REFL}		V_{REFH}	*		*	V
Output Current		−5		+5	*		*	mA
Load Capacitance	No Oscillation		500			*		pF
Short-Circuit Current			±20			*		mA
Short-Circuit Duration	To V_{SS}, V_{CC}, or GND		Indefinite			*		
REFERENCE INPUT								
V_{REFH} Input Range		V_{REFL} +1.25		+10	*		*	V
V_{REFL} Input Range		−10		V_{REFH} − 1.25	*		*	V
Ref High Input Current		−0.5		3.0	*		*	mA
Ref Low Input Current		−3.5		0	*		*	mA
DYNAMIC PERFORMANCE								
Settling Time	To ±0.012%, 20V Output Step		8	10		*	*	µs
Channel-to-Channel Crosstalk	Full-Scale Step		0.25			*		LSB
Digital Feedthrough			2				*	nV-s
Output Noise Voltage	f = 10kHz		65			*		nV/√Hz
DIGITAL INPUT								
Logic Levels								
V_{IH}	$I_{IH} \le ±10µA$	3.325			*			V
V_{IL}	$I_{IL} \le ±10µA$			1.575			*	V
Data Format			Straight Binary			*		
POWER SUPPLY REQUIREMENTS								
V_{CC}		+14.25		+15.75	*		*	V
V_{SS}		−15.75		−14.25	*		*	V
I_{CC}			6	8.5		*	*	mA
I_{SS}		−8	−6		*	*		mA
Power Dissipation			180	250		*	*	mW
TEMPERATURE RANGE								
Specified Performance		−40		+85	*		*	°C

NOTES: (1) LSB means Least Significant Bit; if V_{REFH} equals +10V and V_{REFL} equals −10V, then one LSB equals 4.88mV. (2) All DAC outputs will match within the specified error band. (3) Ideal output voltage does not take into account zero or full-scale error.

SPECIFICATIONS (Single Supply)

At $T_A = -40°C$ to $+85°C$, $V_{CC} = +15V$, V_{SS} = GND, $V_{REFH} = +10V$, $V_{REFL} = 0V$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7714U			DAC7714UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Linearity Error(1)				±2			±1	LSB(2)
Linearity Matching(3)				±2			±1	LSB
Differential Linearity Error				±1			±1	LSB
Monotonicity	T_{MIN} to T_{MAX}	12			*			Bits
Zero-Scale Error	Code = 004_H			±4			*	LSB
Zero-Scale Drift			2			*		ppm/°C
Zero-Scale Matching(3)				±4			±2	LSB
Full-Scale Error	Code = FFF_H			±4			*	LSB
Full-Scale Matching(3)				±4			±2	LSB
Power Supply Sensitivity	At Full Scale		20			*		ppm/V
ANALOG OUTPUT								
Voltage Output(4)		V_{REFL}		V_{REFH}	*		*	V
Output Current		−5		+5	*			mA
Load Capacitance	No Oscillation		500			*		pF
Short-Circuit Current			±20			*		mA
Short-Circuit Duration	To V_{CC} or GND		Indefinite			*		
REFERENCE INPUT								
V_{REFH} Input Range		V_{REFL} +1.25		+10	*		*	V
V_{REFL} Input Range		0		V_{REFH} − 1.25	*		*	V
Ref High Input Current		−0.3		1.5	*		*	mA
Ref Low Input Current		−2.0		0	*		*	mA
DYNAMIC PERFORMANCE								
Settling Time(5)	To ±0.012%, 10V Output Step		8	10		*	*	µs
Channel-to-Channel Crosstalk			0.25			*		LSB
Digital Feedthrough			2				*	nV-s
Output Noise Voltage	f = 10kHz		65			*		nV/√Hz
DIGITAL INPUT/OUTPUT								
Logic Levels								
V_{IH}	$I_{IH} \le ±10µA$	3.325			*			V
V_{IL}	$I_{IL} \le ±10µA$			1.575			*	V
Data Format			Straight Binary			*		
POWER SUPPLY REQUIREMENTS								
V_{CC}		14.25		15.75	*		*	V
I_{CC}			3.0			*	*	mA
Power Dissipation			45			*		mW
TEMPERATURE RANGE								
Specified Performance		−40		+85	*		*	°C

NOTES: (1) If $V_{SS} = 0V$, specification applies at code 004_H and above. (2) LSB means Least Significant Bit; if V_{REFH} equals +10V and V_{REFL} equals 0V, then one LSB equals 2.44mV. (3) All DAC outputs will match within the specified error band. (4) Ideal output voltage does not take into account zero or full-scale error. (5) Full-scale positive 10V step and negative step from code FFF_H to 020_H.

Tournez la page S.V.P.

THEORY OF OPERATION

The DAC7714 is a quad, serial input, 12-bit, voltage output DAC. The architecture is a classic R-2R ladder configuration followed by an operational amplifier that serves as a buffer. Each DAC has its own R-2R ladder network and output op amp, but all share the reference voltage inputs, as shown in Figure 1. The minimum voltage output ("zero-scale") and maximum voltage output ("full-scale") are set by external voltage references (V_{REFL} and V_{REFH}, respectively). The digital input is a 16-bit serial word that contains the 12-bit DAC code and a 2-bit address code that selects one of the four DACs (the two remaining bits are unused). The converter can be powered from a single +15V supply or a dual ±15V supply. Each device offers a reset function which immediately sets all DAC output voltages and internal registers to either zero-scale (code 000_H) or mid-scale (code 800_H). The reset code is selected by the state of the RESETSEL pin (LOW = 000_H, HIGH = 800_H). Figures 2 and 3 show the basic operation of the DAC7714.

ANALOG OUTPUTS

When V_{SS} = –15V (dual supply operation), the output amplifier can swing to within 4V of the supply rails, over the –40°C to +85°C temperature range. With V_{SS} = 0V (single-supply operation), the output can swing to ground. Note that the settling time of the output op amp will be longer with voltages very near ground. Care must also be taken when measuring the zero-scale error when V_{SS} = 0V. If the output amplifier has a negative offset, the output voltage may not change for the first few digital input codes (000_H, 001_H, 002_H, etc.) since the output voltage cannot swing below ground.

At the negative offset limit of –4LSB (–9.76mV), for the single-supply case, the first specified output starts at code 004_H.

REFERENCE INPUTS

The reference inputs, V_{REFL} and V_{REFH}, can be any voltage between V_{SS} – 4V and V_{CC} – 4V provided that V_{REFH} is at least 1.25V greater than V_{REFL}. The minimum output of each D/A is equal to V_{REFL} – 1LSB plus a small offset voltage (essentially, the offset of the output op amp). The maximum output is equal to V_{REFH} plus a similar offset voltage. Note that V_{SS} (the negative power supply) must either be connected to ground or must be in the range of –14.75V to –15.75V. The voltage on V_{SS} sets several bias points within the converter. If V_{SS} is not in one of these two configurations, the bias values may be in error and proper operation of the device is not guaranteed.

The current into the reference inputs depends on the DAC output voltages and can vary from a few microamps to approximately 3mA. The reference input appears as a varying load to the reference. If the reference can sink or source the required current, a reference buffer is not required. See "Reference Current vs Code" in the Typical Performance Curves.

The analog supplies must come up before the reference power supplies, if they are separate. If the power supplies for the references come up first, then the V_{CC} and V_{SS} supplies will be powered from the reference via the ESD protection diodes (see page 4).

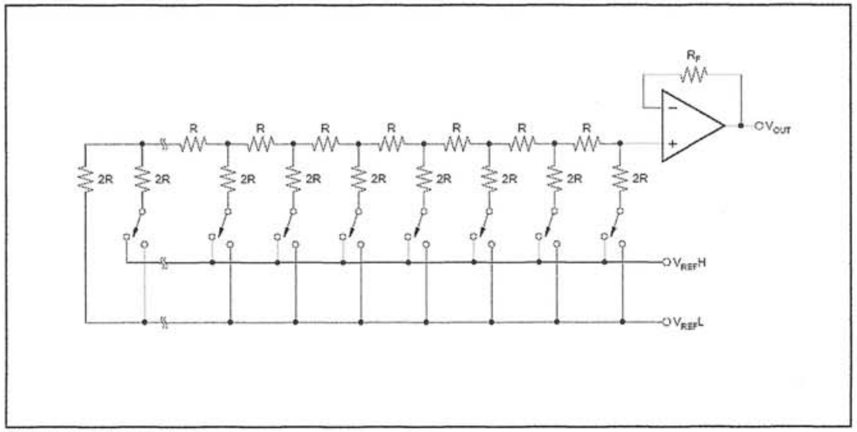


FIGURE 1. DAC7714 Architecture.

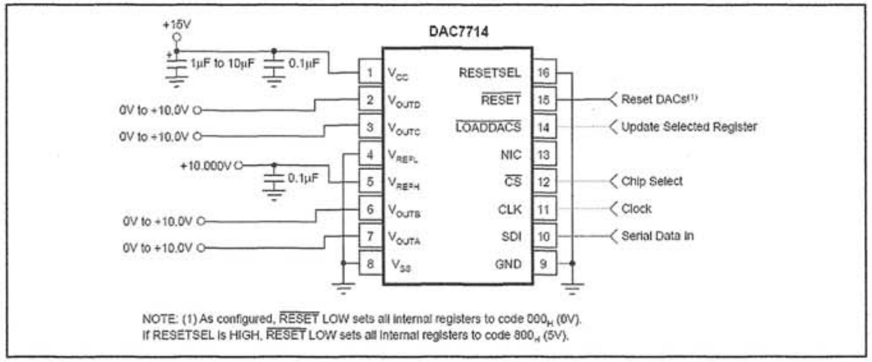


FIGURE 2. Basic Single-Supply Operation of the DAC7714.

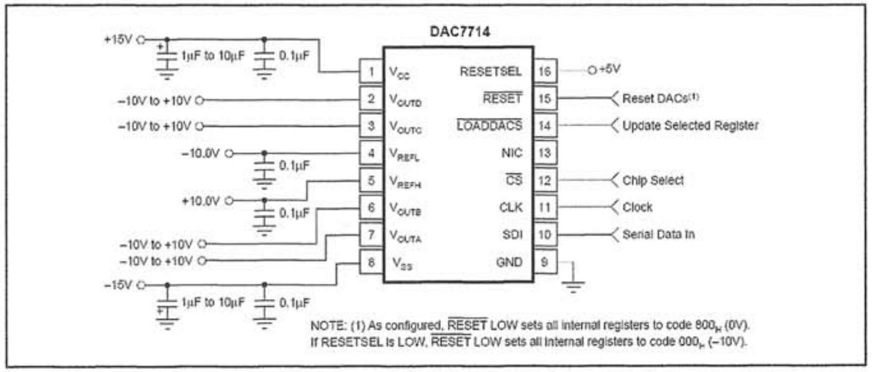


FIGURE 3. Basic Dual-Supply Operation of the DAC7714.

DIGITAL INTERFACE

Figure 4 and Table I provide the basic timing for the DAC7714. The interface consists of a serial clock (CLK), serial data (SDI), and a load DAC signal ($\overline{LOADDACS}$). In addition, a chip select ($\overline{CS}$) input is available to enable serial communication when there are multiple serial devices. An asynchronous reset input ($\overline{RESET}$) is provided to simplify start-up conditions, periodic resets, or emergency resets to a known state.

The DAC code and address are provided via a 16-bit serial interface (see Figure 4). The first two bits select the DAC register that will be updated when $\overline{LOADDACS}$ goes LOW (see Table II). The next two bits are not used. The last 12 bits is the DAC code which is provided, most significant bit first.

Note that $\overline{CS}$ and CLK are combined with an OR gate and the output controls the serial-to-parallel shift register internal to the DAC7714 (see the block diagram on the front of this data sheet). These two inputs are completely interchangeable. In addition, care must be taken with the state of CLK when $\overline{CS}$ rises at the end of a serial transfer. If CLK is LOW when $\overline{CS}$ rises, the OR gate will provide a rising edge to the shift register, shifting the internal data one additional bit. The result will be incorrect data and possible selection of the wrong DAC.

If both $\overline{CS}$ and CLK are used, then $\overline{CS}$ should rise only when CLK is HIGH. If not, then either $\overline{CS}$ or CLK can be used to operate the shift register. See Table III for more information.

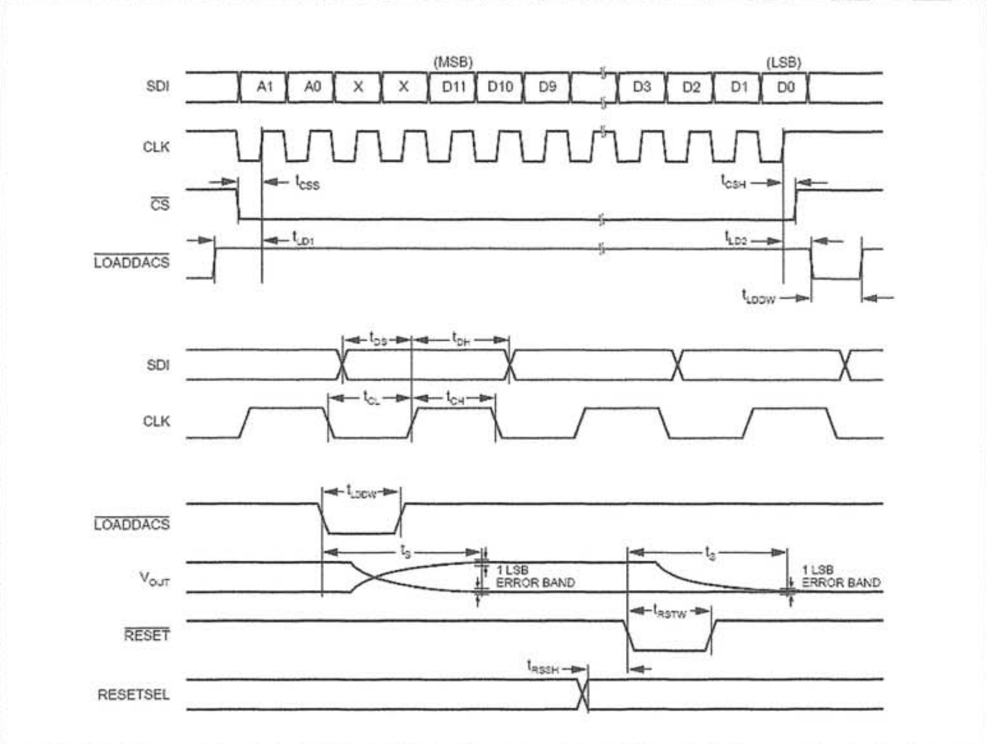


FIGURE 4. DAC7714 Timing.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{DS}	Data Valid to CLK Rising	25			ns
t_{DH}	Data Held Valid after CLK Rises	20			ns
t_{CH}	CLK HIGH	30			ns
t_{CL}	CLK LOW	50			ns
t_{CSS}	CS LOW to CLK Rising	55			ns
t_{CSH}	CLK HIGH to CS Rising	15			ns
t_{LD1}	LOADDACS HIGH to CLK Rising	40			ns
t_{LD2}	CLK Rising to LOADDACS LOW	15			ns
t_{LDDW}	LOADDACS LOW Time	45			ns
t_{RSSH}	RESETSEL Valid to RESET LOW	25			ns
t_{RSTW}	RESET LOW Time	70			ns
t_S	Settling Time	10			µs

TABLE I. Timing Specifications (T_A = –40°C to +85°C).

A1	A0	LOADDACS	RESET	SELECTED DAC REGISTER	STATE OF SELECTED DAC REGISTER
L(1)	L	L	H(2)	A	Transparent
L	H	L	H	B	Transparent
H	L	L	H	C	Transparent
H	H	L	H	D	Transparent
X(3)	X	H	H	NONE	(All Latched)
X	X	X	L	ALL	Reset(4)

NOTES: (1) L = Logic LOW. (2) H = Logic HIGH. (3) X = Don't Care. (4) Resets to either 000H or 800H per the RESETSEL state (LOW = 000H, HIGH = 800H). When RESET rises, all registers that are in their latched state retain the reset value.

TABLE II. Control Logic Truth Table.

Integrated
Circuit
Systems, Inc.

AV9173-01

Video Genlock PLL

General Description

The **AV9173-01** provides the analog circuit blocks required for implementing a video genlock dot (pixel) clock generator. It contains a phase detector, charge pump, loop filter, and voltage-controlled oscillator (VCO). By grouping these critical analog blocks into one IC and utilizing external digital functions, performance and design flexibility are optimized as are development time and system cost.

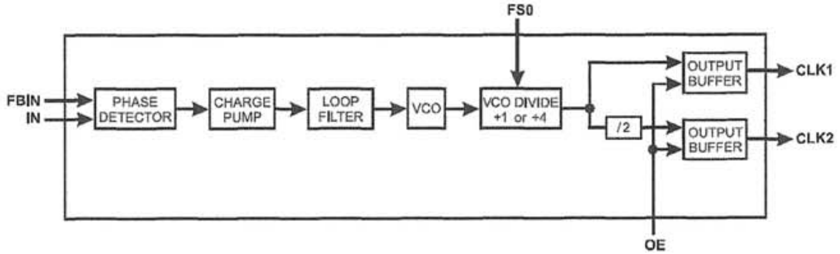
When used with an external clock divider, the **AV9173-01** forms a Phase-Locked Loop configured as a frequency synthesizer. The **AV9173-01** is designed to accept video horizontal synchronization (h-sync) pulses and produce a video dot clock. A separated, negative-going sync input reference pulse is required at pin 2 (IN).

The **AV9173-01** is also suited for other clock recovery applications in such areas as data communications.

Features

- Phase-detector/VCO circuit block
- Ideal for genlock system
- Reference clock range 25kHz to 1MHz for full output clock range
- Input clocks down to 12 kHz possible with restricted output conditions (see Table 1)
- Output clock range 1.25 to 75MHz
- On-chip loop filter
- Single 5 volt power supply
- Low power CMOS technology
- Small 8-pin DIP or SOIC package

Block Diagram



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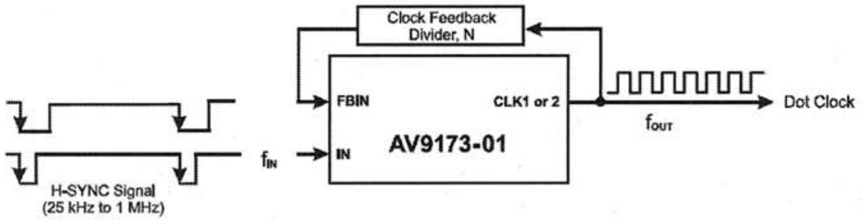
Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	FBIN	Input	Feedback Input
2	IN	Input	Input for reference sync pulse
3	GND	—	Ground
4	FS0	Input	Frequency Select 0 input
5	OE	Input	Output Enable
6	CLK1	Output	Clock Output 1
7	VDD	—	Power Supply (+5V)
8	CLK2	Output	Clock Output 2 (Divided-by-2 from Clock 1)

Table 1: Allowable Input Frequency to Output Frequency (Outputs in MHz)

f_{IN} (kHz)	f_{OUT} for FS = 0 (MHz)		f_{OUT} for FS = 1 (MHz)	
	CLK1 Output	CLK2 Output	CLK1 Output	CLK2 Output
$12 \le f_{IN} \le 14$ kHz	44.0 to 75	22.0 to 37.5	11.0 to 18.75	5.5 to 9.375
$14 < f_{IN} \le 17$ kHz	30.0 to 75	15.0 to 37.5	7.5 to 18.75	3.75 to 9.375
$17 < f_{IN} \le 30$ kHz	25.0 to 75	12.5 to 37.5	6.25 to 18.75	3.125 to 9.375
$30 < f_{IN} \le 35$ kHz	15.0 to 75	7.5 to 37.5	3.75 to 18.75	1.875 to 9.375
$35 < f_{IN} \le 1000$ kHz	10.0 to 75	5.0 to 37.5	2.5 to 18.75	1.25 to 9.375

Figure 1: Typical Application of AV9173-01 in a Video Genlock System



Using the AV9173-01

Most video sources, such as video cameras, are asynchronous, free-running devices. To digitize video or synchronize one video source to another free-running reference video source, a video "genlock" (generator lock) circuit is required. The **AV9173-01** integrates the analog blocks which make the task much easier.

In the complete video genlock circuit, the primary function of the **AV9173-01** is to provide the analog circuitry required to generate the video dot clock within a PLL. This application is illustrated in Figure 1. The input reference signal for this circuit is the horizontal synchronization (h-sync) signal. If a composite video reference source is being used, the h-sync pulses must be separated from the composite signal. A video sync separator circuit, such as the National Semiconductor LM1881, can be used for this purpose.

The clock feedback divider shown in Figure 1 is a digital divider used within the PLL to multiply the reference frequency. Its divide ratio establishes how many video dot clock cycles occur per h-sync pulse. For example, if 880 pixel clocks are desired per h-sync pulse, then the divider ratio is set to 880. Hence, together the h-sync frequency and external divider ratio establish the dot clock frequency:

$f_{OUT} = f_{IN} \cdot N$ where N is external divide ratio

Both **AV9173-01** input pins IN and FBIN respond only to negative-going clock edges of the input signal. The h-sync signal must be constant frequency in the 25 kHz to 1 MHz range and stable (low clock jitter) for creation of a stable output clock.

Refer to Application Brief (AB01) for additional details on use of input frequencies below 25kHz. By following the guidelines in this brief and meeting the test conditions in the AC specifications (VCO frequency), an input as low as 12kHz (such as NTSC or PAL h-sync) can be used.

The output hook-up of the **AV9173-01** is dictated by the desired dot clock frequency. The primary consideration is the internal VCO which operates over a frequency range of 10 MHz to 75 MHz. Because of the selectable VCO output divider and the additional divider on output CLK2, four distinct output frequency ranges can be achieved. The following Table lists these ranges and the corresponding device configuration.

FS0 State	Output Used	Frequency Range
0	CLK1	10 - 75 MHz
0	CLK2	5 - 37.5 MHz
1	CLK1	2.5 - 18.75 MHz
1	CLK2	1.25 - 9.375 MHz

Note that both outputs, CLK1 and CLK2, are available during operation even though only one is fed back via the external clock divider.

Pin 5, OE, tristates both CLK1 and CLK2 upon logic low input. This feature can be used to revert dot clock control to the system clock when not in genlock mode (hence, when in genlock mode the system dot clock must be tristated).

When unused, inputs FS0 and OE must be tied to either GND (logic low) or VDD (logic high).

For further discussion of VCO/PLL operation as it applies to the **AV9173-01**, please refer to the AV9170 application note. The AV9170 is a similar device with fixed feedback dividers for skew control applications.

PRODUCT SPECIFICATIONS

SHARP

AVC Liquid Crystal Displays Group

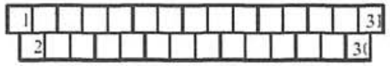
LQ104V1DG51

TFT-LCD Module

4. Input Terminals

4-1. TFT-LCD panel driving

CN1 Used connector:DF9MA-31P-1V (Hirose Electric Co., Ltd.)



Corresponding connector: DF9-31S-1V (〃)

DF9A-31S-1V(〃)

DF9B-31S-1V(〃)

DF9M-31S-1V(〃)

CN1 pin arrangement from module surface
(Transparent view)

Pin No.	Symbol	Function	Remark
1	GND		
2	CK	Clock signal for sampling each data signal	
3	Hsync	Horizontal synchronous signal	【Note1】
4	Vsync	Vertical synchronous signal	【Note1】
5	GND		
6	R0	RED data signal(LSB)	
7	R1	RED data signal	
8	R2	RED data signal	
9	R3	RED data signal	
10	R4	RED data signal	
11	R5	RED data signal(MSB)	
12	GND		
13	G0	GREEN data signal(LSB)	
14	G1	GREEN data signal	
15	G2	GREEN data signal	
16	G3	GREEN data signal	
17	G4	GREEN data signal	
18	G5	GREEN data signal(MSB)	
19	GND		
20	B0	BLUE data signal(LSB)	
21	B1	BLUE data signal	
22	B2	BLUE data signal	
23	B3	BLUE data signal	
24	B4	BLUE data signal	
25	B5	BLUE data signal(MSB)	
26	GND		
27	ENAB	Signal to settle the horizontal display position	【Note2】
28	Vcc	+3.3/5.0V power supply	
29	Vcc	+3.3/5.0V power supply	
30	R/L	Horizontal display mode select signal	【Note3】
31	U/D	Vertical display mode select signal	【Note4】

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6. Electrical Characteristics

6-1.TFT-LCDpaneldriving

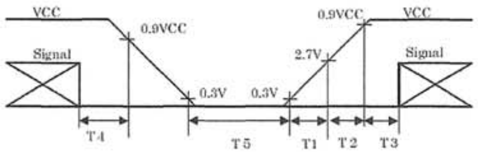
Ta=25℃

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Power Supply	Supply voltage	Vcc	+3.0	+3.3 / +5.0	+5.5	V	【Note1】
	Current dissipation	Icc	—	180	270	mA	Vcc=3.3V 【Note2】
		Icc	—	150	230	mA	Vcc=5.0V 【Note2】
Permissive input ripple voltage		V_{RF}	—	—	100	mVp-p	
Input voltage (Low)		V_{IL}	—	—	0.3Vcc	V	
Input voltage (High)		V_{IH}	0.7Vcc	—	—	V	【Note3】
Input current (low)		I_{OL1}	—	—	1.0	μA	V_I=0V 【Note4】
		I_{OL2}			10	μA	V_I=0V 【Note5】
		I_{OL3}	-	-	800	μA	V_I=0V 【Note6】
Input current (High)		I_{OH1}	—	—	1.0	μA	V_I=Vcc 【Note7】
		I_{OH2}			300	μA	V_I=Vcc 【Note8】
		I_{OH3}	—	—	800	μA	V_I=Vcc 【Note9】

【 NOTE 1】

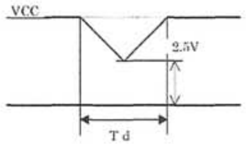
Vcc-turn-on conditions

$0 < T1 \leq 15ms$
$0 < T2 \leq 10ms$
$0 < T3 \leq 100ms$
$0 < T4 \leq 1s$
$T5 > 200ms$

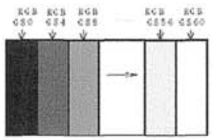


Vcc-dip conditions

1) $2.5V \leq Vcc$
$td \leq 10ms$
2) $Vcc < 2.5V$
Vcc-dip condition should also follow
The Vcc-turn-on conditions



【Note2】 Typical current situation : 16-gray-bar pattern.
480 line mode/Vcc=+3.3V/+5.0V



【Note3】 CK,R0~R5,G0~G5,B0~B5,Hsync,Vsync,ENAB, R/L,U/D

【Note4】 CK,R0~R5,G0~G5,B0~B5,Hsync,Vsync,

【Note5】 U/D,ENAB

【Note6】 R/L

【Note7】 CK,R0~R5,G0~G5,B0~B5,Hsnc,Vsync,R/L

【Note8】 ENAB

【Note9】 U/D

7. Timing Characteristics of input signals

Timing diagrams of input signal are shown in Fig.2 - ①~③ .

7-1. Timing characteristics

Parameter		Symbol	Mode	Min.	Typ.	Max.	Unit	Remark
Clock	Frequency	1/Tc	all	—	25.18	28.33	MHz	
	High time	Tch	〃	5	—	—	ns	
	Low time	Tcl	〃	10	—	—	ns	
Data	Setup time	Tds	〃	5	—	—	ns	
	Hold time	Tdh	〃	10	—	—	ns	
Horizontal sync. signal	Cycle	TH	〃	30.00	31.78	—	μs	
			〃	750	800	900	clock	
	Pulse width	THp	〃	2	96	200	clock	
Vertical sync. signal	Cycle	TV	480	515	525	560	line	
			400	446	449	480	line	
			350	447	449	510	line	
	Pulsewidth	TVp	all	1	—	34	line	
Horizontal display period		THd	〃	640	640	640	clock	
Hsync-Clock phase difference		THc	〃	10	—	Tc-10	ns	
Hsync-Vsync phase difference		TVh	〃	0	—	TH-THp	clock	

Note) In case of lower frequency, the deterioration of display quality, flicker etc.,may be occurred.

7-2. Horizontal display position

The horizontal display position is determined by ENAB signal and the input data corresponding to the rising edge of ENAB signal is displayed at the left end of the active area.

Parameter		symbol	Min.	Typ.	Max.	Unit	Remark
Enable signal	Setup time	Tes	5	—	Tc-10	ns	
	Pulse width	Tep	2	640	640	clock	
Hsync-Enable signal phase difference		THe	44	—	TH-664	clock	

Note) When ENAB is fixed "Low", the display starts from the data of C104(clock) as shown in Fig.2-①~③. Be careful that the module does not work when ENAB is fixed "High". When the phase difference is below 104 clock, keep the "High level of ENAB is signal longer Than 104-The. If it will not be keeped, the display starts from the data of C104(clock).

7-3. Vertical display position

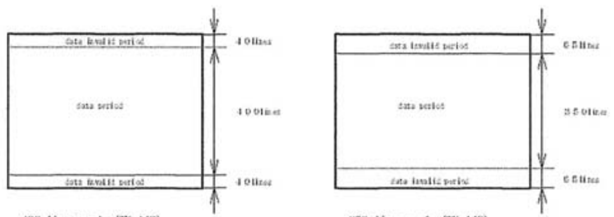
The vertical display position is automatically centered in the active area at each mode of VGA ,480-,400-,and 350-line mode . Each mode is selected depending on the polarity of the synchronous signals described in 4-1(Note1).

In each mode ,the data of TVn is displayed at the top line of the active area. And the display position will be centered on the screen like the following figure when the period of vertical synchronous signal,TV,is typical value.

In 400-,and 350-line mode,the data in the vertical data invalid period is also displayed, So ,inputting all data "0" is recommended during vertical data invalid period.

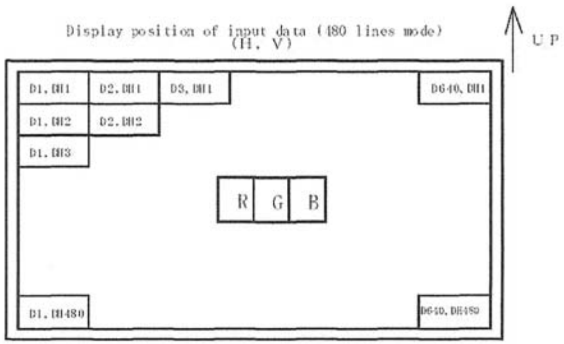
ENAB signal has no relation to the vertical display position.

Mode	V-data start(TVs)	V-data period(TVd)	V-display start(TVn)	V-display period	Unit	Remark
480	34	480	34	480	line	
400	34	400	443-TV	480	line	
350	61	350	445-TV	480	line	



400 lines mode (TV=449) 350 lines mode (TV=449)

7-4. Input Data Signals and Display Position on the screen



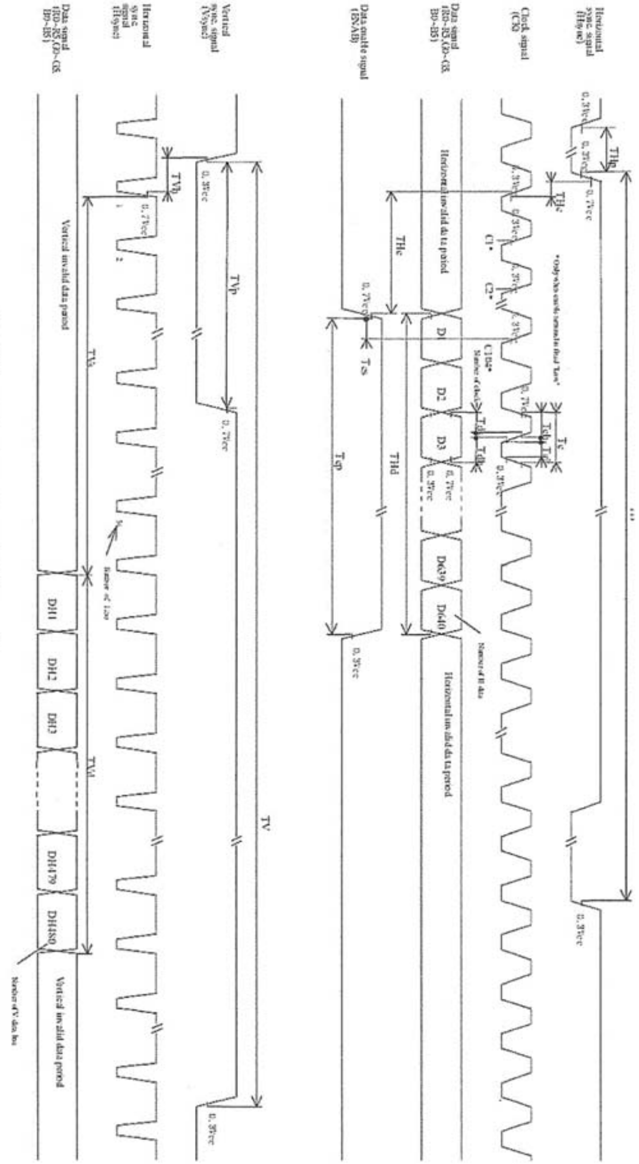


Fig 2-1 Input signal waveforms (480 line mode)

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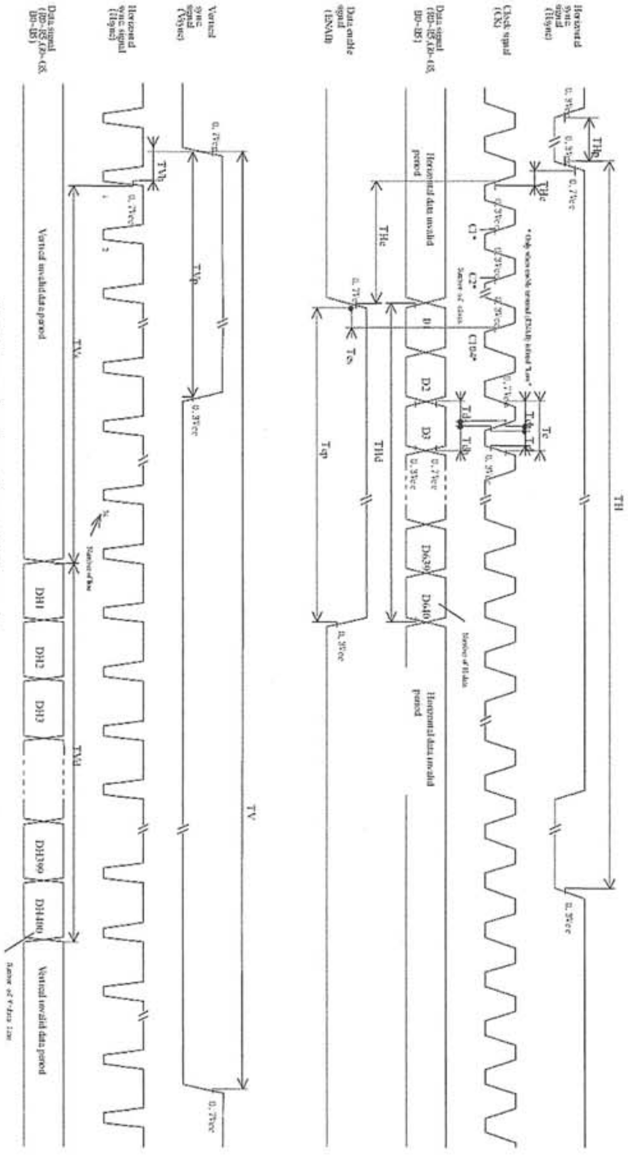

Fig.2-2 Input signal waveforms (400 line mode)

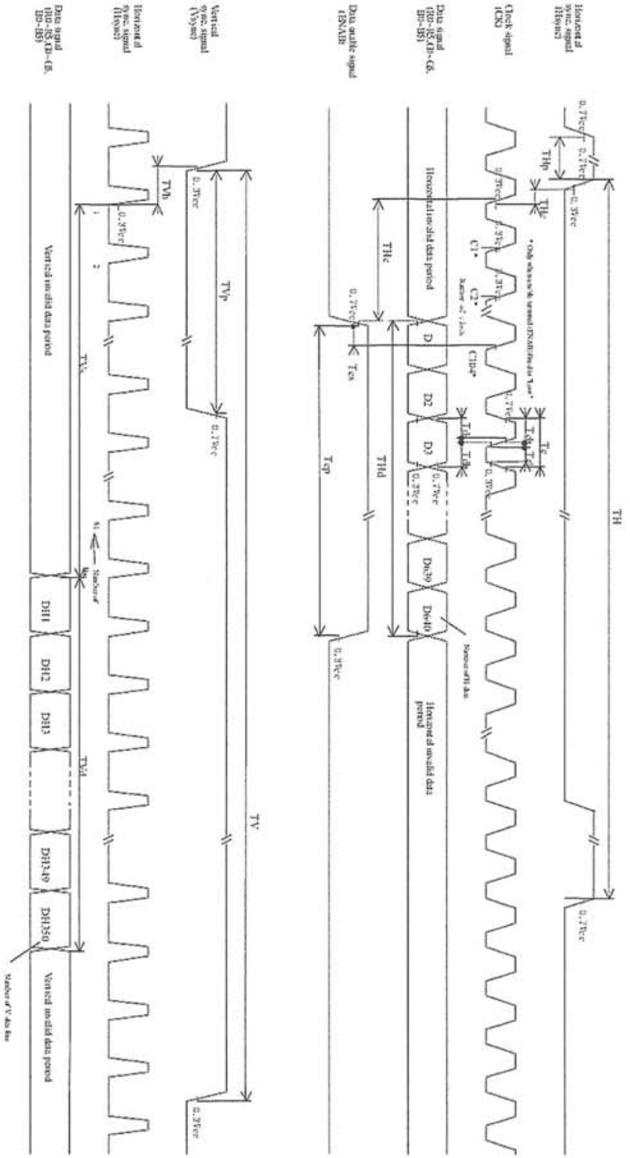

Fig.2-3 Input signal waveforms (350 line mode)

8. Input Signals, Basic Display Colors and Gray Scale of Each Color

	Colors & Gray scale	Gray Scale	R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	B5
Basic Color	Black	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	—	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Green	—	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Cyan	—	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Red	—	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	—	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	—	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	—	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓			↓						↓						↓			
	⇩	↓			↓						↓						↓			
	Brighter	GS61	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	⇩	GS62	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS63	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	⇧	↓			↓						↓						↓			
	⇩	↓			↓						↓						↓			
	Brighter	GS61	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0
	⇩	GS62	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
	Green	GS63	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale of Blue	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
	⇧	↓			↓						↓						↓			
	⇩	↓			↓						↓						↓			
	Brighter	GS61	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1
	⇩	GS62	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	Blue	GS63	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

0 :Low level voltage, 1 : High level voltage

Each basic color can be displayed in 64 gray scales from 6 bit data signals. According to the combination of total 18 bit data signals, the 262,144-color display can be achieved on the screen.

9. Optical Characteristics

Ta=25℃, Vcc=+5V

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle Range	Horizontal	θ21, θ22	CR > 10	60	70	—	Deg.	【Note1,4】
	Vertical	θ11		35	40	—	Deg.	
		θ12		55	70	—	Deg.	
Contrast ratio		CR	θ=0°	150	—	—	—	【Note2,4】
			Optimum Viewing Angle	—	300	—	—	
Response Time	Rise	τr	θ=0°	—	20	—	ms	【Note3,4】
	Decay	τd		—	40	—	ms	
Chromaticity of White		x		—	0.313	—		【Note4】
		y		—	0.329	—		I_L=6.0mArms
Luminance of white		Y_L		280	350	—	cd/m²	f=60kHz
White Unifomity		δw		—	—	1.45	—	【Note5】
Viewing Angle range as a Brightness Definition	Horizontal	θ21, θ22	50% of the maximum brightness	—	45	—	Deg.	【Note1】
	Vertical	θ11		—	35	—	Deg.	
		θ12		—	35	—	Deg.	

※The measurement shall be executed 30 minutes after lighting at rating. (condition:I_L=6.0mArms)

The optical characteristics shall be measured in a dark room or equivalent state with the method shown in Fig.3 below.

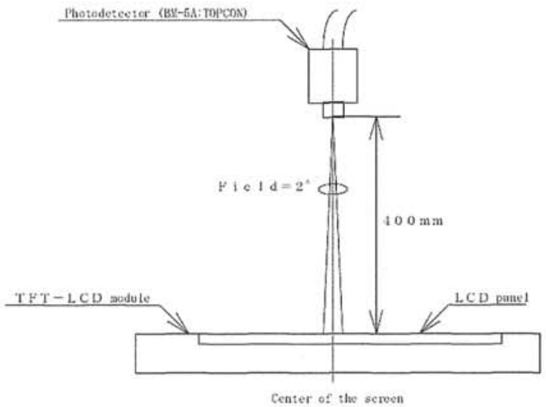

Fig.3 Optical characteristics measurement method