NE RIEN ÉCRIRE DANS CE CADRE

MINISTÈRE DE L'ÉDUCATION NATIONALE

Académie : Session :

Concours :

Spécialité/option : Repère de l'épreuve :

Intitulé de l'épreuve :

NOM :
(en majuscules, suivi s'il y a lieu, du nom d'épouse)

Prénoms : N° du candidat

(le numéro est celui qui figure sur la convocation ou la liste d'appel)

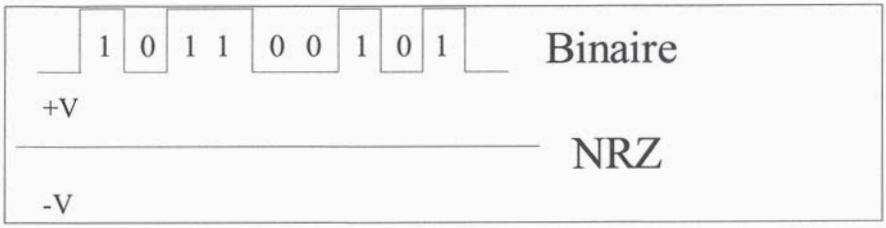
EAI GEA 1

Document réponse DR1

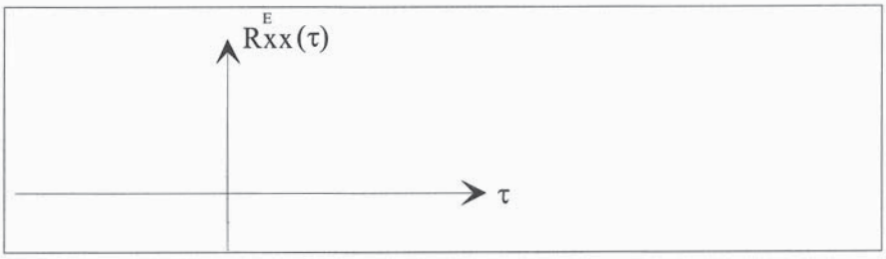
Question 5-1-2

Signal	Etat
Frame 10/20	
SDCLK/8Khz	
ModTRI/SQ	
LI SENS/2.048 Mhz	
RE2/BCLK	
Master/Slave	

Question 6-4-1



Question 6-4-3



D

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MINISTÈRE DE L'ÉDUCATION NATIONALE

Académie : Session :

Concours :

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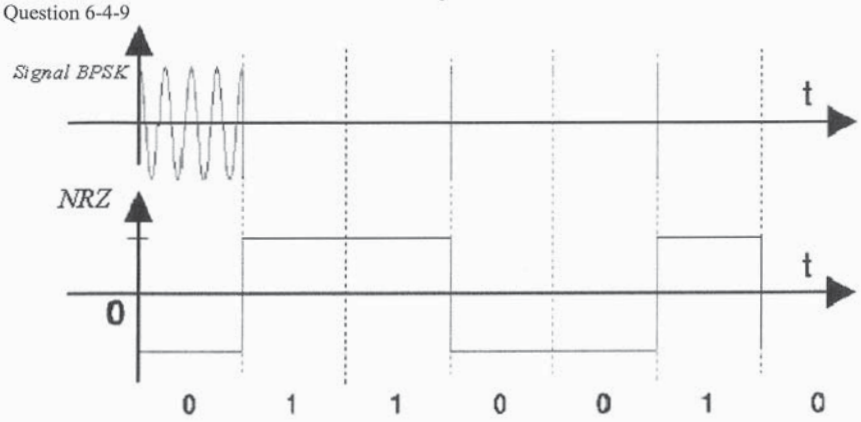
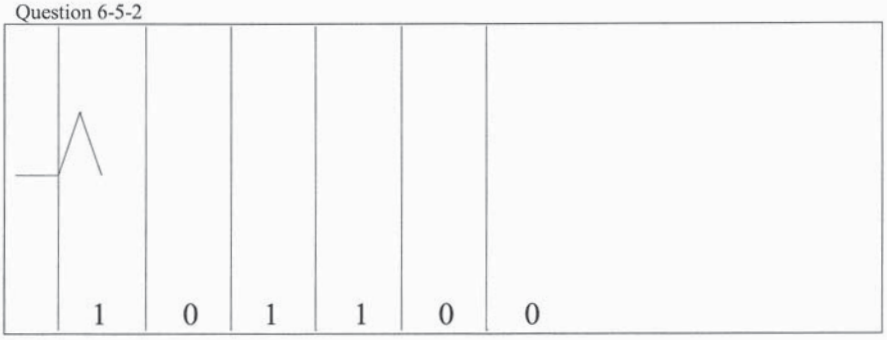
EAI GEA 1

Document réponse DR2

Question 6-4-9



Question 6-5-2



Question 6-5-3

E

NE RIEN ÉCRIRE DANS CE CADRE

MINISTÈRE DE L'ÉDUCATION NATIONALE

Académie : Session :

Concours :

Spécialité/option : Repère de l'épreuve :

Intitulé de l'épreuve :

NOM :
(en majuscules, suivi s'il y a lieu, du nom d'épouse)

Prénoms : N° du candidat

(le numéro est celui qui figure sur la convocation ou la liste d'appel)

EAI GEA 1

Document réponse DR3

Question 6-5-5

F

Documents constructeurs

Tournez la page S.V.P.

intersil

HC-5504B

Data Sheet | March 2003 | FN2886.7

EIA/ITU PABX SLIC with 40mA Loop Feed

The Intersil SLIC incorporates many of the BORSHT functions on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. This device is designed to maintain transmission performance in the presence of externally induced longitudinal currents. Using the unique Intersil dielectric isolation process, the SLIC can operate directly with a wide range of station battery voltages.

The SLIC also provides selective denial of power. If the PBX system becomes overloaded during an emergency, the SLIC will provide system protection by denying power to selected subscriber loops.

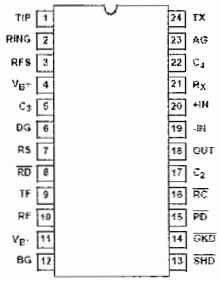
The Intersil SLIC is ideally suited for the design of new digital PBX systems by eliminating bulky hybrid transformers.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HC9P5504B-5	0 to 75	24 Ld SOIC	M24.3

Pinout

HC-5504B (SOIC)
TOP VIEW



Features

- Pin for Pin Replacement for the HC-5504
- Capable of 5V or 12V (V_{B+}) Operation
- Monolithic Integrated Device
- DI High Voltage Process
- Compatible With Worldwide PBX Performance Requirements
- Controlled Supply of Battery Feed Current for Short Loops (41mA)
- Internal Ring Relay Driver
- Allows Interfacing With Negative Superimposed Ringing Systems
- Low Power Consumption During Standby
- Switch Hook Ground Key and Ring Trip Detection Functions
- Selective Denial of Power to Subscriber Loops

Applications

- Solid State Line Interface Circuit for Analog and Digital PBX Systems
- Direct Inward Dial (DID) Trunks
- Voice Messaging PBXs
- Related Literature
  - AN549, The HC-5502S/4X Telephone Subscriber Line Interface Circuits (SLIC)
  - AN571, Using Ring Sync with HC-5502A and HC-5504 SLICs

Absolute Maximum Ratings (Note 1)

Maximum Continuous Supply Voltages
- (V_{B-}) ..... -60V to 0.5V
- (V_{B+}) ..... -0.5V to 15V
- (V_{B+} - V_{B-}) 75V

Relay Drive Voltage (V_{RD}) ..... -0.5V to 15V

Operating Conditions

Operating Temperature Range
- HC-5504B-5 ..... 0^oC to 75^oC

Relay Driver Voltage (V_{RD}) ..... 5 to 12V
Positive Supply Voltage (V_{B+}) ..... 4.75 to 5.25 or 10.8 to 13.2V
Negative Supply Voltage (V_{B-}) ..... -42 to -56V
High Level Logic Input Voltage 2.4V
Low Level Logic Input Voltage 0.6V
Loop Resistance (R_L) ..... 200 to 1200Ω

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} ($^oC/W$)
- SOIC Package 75

Maximum Junction Temperature (Plastic Packages) ..... 150^oC
Maximum Storage Temperature Range ..... -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) ..... 300^oC
(SOIC - Lead Tips Only)

Die Characteristics

Transistor Count 185
Diode Count 36
Die Dimensions ..... 137 x 102
Substrate Potential ..... Connected
Process ..... Bipolar-DI

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Unless Otherwise Specified, V_{B-} = -48V, V_{B+} = 12V and 5V, AG = BG = DG = 0V, Typical Parameters T_A = 25^oC. Min-Max Parameters are Over Operating Temperature Range

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On Hook Power Dissipation	I_{LONG} = 0 (Note 3), V_{B+} = 12V	-	170	235	mW
Off Hook Power Dissipation	R_L = 600Ω, I_{LONG} = 0 (Note 3), V_{B+} = 12V	-	425	550	mW
Off Hook I_{B+}	R_L = 600Ω, I_{LONG} = 0 (Note 3), T_A = -40^oC	-	-	6.0	mA
Off Hook I_{B+}	R_L = 600Ω, I_{LONG} = 0 (Note 3), T_A = 25^oC	-	-	5.3	mA
Off Hook I_{B-}	R_L = 600Ω, I_{LONG} = 0 (Note 3)	-	35	41	mA
Off Hook Loop Current	R_L = 1200Ω, I_{LONG} = 0 (Note 3)	-	21	-	mA
Off Hook Loop Current	R_L = 1200Ω, V_{B-} = -42V, I_{LONG} = 0 (Note 3) T_A = 25^oC	17.5	-	-	mA
Off Hook Loop Current	R_L = 200Ω, I_{LONG} = 0 (Note 3)	36	41	48	mA
Fault Currents					
TIP to Ground		-	14	-	mA
RING to Ground		-	55	-	mA
TIP to RING		-	41	-	mA
TIP and RING to Ground		-	55	-	mA
Ring Relay Drive V_{OL}	I_{OL} = 62mA	-	0.2	0.5	V
Ring Relay Driver Off Leakage	V_{RD} = 12V, $\overline{RC}$ = 1 = HIGH, T_A = 25^oC	-	-	100	µA
Ring Trip Detection Period	R_L = 600Ω	-	2	3	Ring Cycles
Switch Hook Detection Threshold	$\overline{SHD}$ = V_{OL}	10	-	-	mA
	$\overline{SHD}$ = V_{OH}	-	-	5	mA
Ground Key Detection Threshold	$\overline{GKD}$ = V_{OL}	20	-	-	mA
	$\overline{GKD}$ = V_{OH}	-	-	10	mA

Electrical Specifications Unless Otherwise Specified, V_B- = -48V, V_B+ = 12V and 5V, AG = BG = DG = 0V, Typical Parameters T_A = 25°C. Min-Max Parameters are Over Operating Temperature Range (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Loop Current During Power Denial	R_L = 200Ω	-	±2	-	mA
Dial Pulse Distortion		0	-	5	ms
Receive Input Impedance	(Note 3)	-	110	-	kΩ
Transmit Output Impedance	(Note 3)	-	10	20	Ω
2-Wire Return Loss	Referenced to 600Ω + 2.16µF (Note 3)				
SR_L LO		-	15.5	-	dB
ER_L		-	24	-	dB
SR_L HI		-	31	-	dB
Longitudinal Balance	$1V_{RMS}$ 200Hz - 3400Hz (Note 2) IEEE Method				
2-Wire Off Hook	$0°C \le T_A \le 75°C$	58	65	-	dB
2-Wire On Hook		60	63	-	dB
4-Wire Off Hook		50	56	-	dB
Low Frequency Longitudinal Balance	R.E.A. Method (Note 3), R_L = 600Ω	-	-	23	dBrnC
	$0°C \le T_A \le 75°C$	-	-	-67	dBm0p
Insertion Loss	at 1kHz, 0dBm Input Level. Referenced 600Ω				
2-Wire to 4-Wire, 4 Wire to 2-Wire		-	±0.05	±0.2	dB
Frequency Response	200Hz - 3400Hz Referenced to Absolute Loss at 1kHz and 0dBm Signal Level (Note 3)	-	±0.02	±0.05	dB
Idle Channel Noise	(Note 3)				
2-Wire to 4-Wire, 4 Wire to 2-Wire		-	1	5	dBrnC
		-	-89	-85	dBm0p
Absolute Delay	(Note 3)				
2-Wire to 4-Wire, 4 Wire to 2-Wire		-	-	2	ms
Trans Hybrid Loss	Balance Network Set Up for 600Ω Termination at 1kHz	36	40	-	dB
Overload Level	V_B+ = +5V	1.5	-	-	V_{PEAK}
2-Wire to 4-Wire, 4 Wire to 2-Wire	V_B+ = 12V	1.75	-	-	V_{PEAK}
Level Linearity	At 1kHz Referenced to 0dBm Level (Note 3)				
2-Wire to 4-Wire, 4 Wire to 2-Wire	+3 to -40dBm	-	-	±0.05	dB
	-40 to -50dBm	-	-	±0.1	dB
	-50 to -55dBm	-	-	±0.3	dB
Power Supply Rejection Ratio	(Note 3)				
V_B+ to 2-Wire	30 - 60Hz, R_L = 600Ω	15	-	-	dB
V_B+ to Transmit		15	-	-	dB
V_B- to 2-Wire		15	-	-	dB
V_B- to Transmit		15	-	-	dB

HC-5504B

Electrical Specifications Unless Otherwise Specified, V_B- = -48V, V_B+ = 12V and 5V, AG = BG = DG = 0V, Typical Parameters T_A = 25°C. Min-Max Parameters are Over Operating Temperature Range (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_B+ to 2-Wire	200 - 16kHz, R_L = 600Ω	30	-	-	dB
V_B+ to Transmit		30	-	-	dB
V_B- to 2-Wire		30	-	-	dB
V_B- to Transmit		30	-	-	dB
Logic Input Current (RS, $\overline{RC}$, $\overline{PD}$)	$0V \le V_{IN} \le 5V$	-	-	±100	µA
Logic Inputs					
Logic '0' V_{IL}		-	-	0.8	V
Logic '1' V_{IH}		2.0	-	5.5	V
Logic Outputs					
Logic '0' V_{OL}	I_{LOAD} 800µA, V_B+ = 12V, 5V	-	0.1	0.5	V
Logic '1' V_{OH}	I_{LOAD} 80µA, V_B+ = 12V	2.7	5.0	5.5	V
	I_{LOAD} 40µA, V_B+ = 5V	2.7	-	5.0	V

Uncommitted Op Amp Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Input Bias Current		-	20	-	nA
Differential Input Resistance	(Note 3)	-	1	-	MΩ
Output Voltage Swing	R_L = 10K, V_B+ = 12V	-	±6.2	±6.6	V_{PEAK}
	R_L = 10K, V_B+ = 5V	-	±3	-	V_{PEAK}
Output Resistance	A_{VCL} = 1 (Note 3)	-	10	-	Ω
Small Signal GBW	(Note 3)	-	1	-	MHz

NOTES:

3. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.
4. I_{LONG} = Longitudinal Current.

Tournez la page S.V.P.

Pin Descriptions

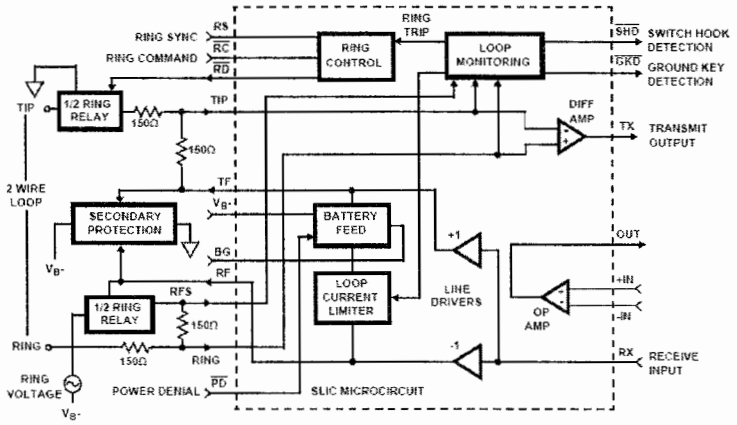
24 PIN SOIC	SYMBOL	DESCRIPTION
1	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Ring terminal to receive voice signals from the telephone and for loop monitoring purposes.
2	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Tip terminal to receive voice signals from the telephone and for loop monitoring purposes.
3	RFS	Senses ring side of loop for ground key and ring trip detection. During ringing, the ring signal is inserted into the line at this node and RF is isolated from RFS via a relay.
4	V_B+	Positive Voltage Source - Most positive supply. V_B+ is typically 12V or 5V.
5	C_3	Capacitor #3 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering V_B-. Typical value is 0.3µF, 30V.
6	DG (Note 5)	Digital Ground - To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC microcircuit.
7	RS	Ring Synchronization Input - A TTL-compatible clock input. The clock should be arranged such that a positive pulse transition occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring relay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to 5V.
8	$\overline{RD}$	Relay Driver - A low active open collector logic output. When enabled, the external ring relay is energized.
9	TF	Tip Feed - A low impedance analog output connected to the TIP terminal through a 150Ω feed resistor. Functions with the RF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
10	RF	Ring Feed - A low impedance analog output connected to the RING terminal through a 150Ω feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
11	V_B-	Negative Voltage Source - Most negative supply. V_B- is typically -48V with an operational range of -42V to -58V. Frequently referred to as "battery".
12	BG (Note 5)	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
13	$\overline{SHD}$	Switch Hook Detection - A low active LS TTL - compatible logic output. This output is enabled for loop currents exceeding 10mA and disabled for loop currents less than 5mA.
14	$\overline{GKD}$	Ground Key Detection - A low active LS TTL - compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 20mA, and disabled if this current difference is less than 10mA.
15	$\overline{PD}$	Power Denial - A low active TTL - Compatible logic input. When enabled, the switch hook detect ($\overline{SHD}$) and ground key detect ($\overline{GKD}$) are not necessarily valid, and the relay driver ($\overline{RD}$) output is disabled.
16	$\overline{RC}$	Ring Command - A low active TTL - Compatible logic input. When enabled, the relay driver ($\overline{RD}$) output goes low on the next high level of the ring sync (RS) input, as long as the SLIC is not in the power denial state ($\overline{PD}$ = 0) or the subscriber is not already off- hook ($\overline{SHD}$ = 0).
17	C_2	Capacitor #2 - An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occurring during ring trip detection. Typical value is 0.15µF, 10V. This capacitor is not used if ground key function is not required and (Pin 17) may be left open or connected to digital ground.
18	OUT	The analog output of the spare operational amplifier. The output voltage swing is typically ±5V.
19	-IN	The inverting analog input of the spare operational amplifier.
20	+IN	The non-inverting analog input of the spare operational amplifier.

HC-5504B

Pin Descriptions (Continued)

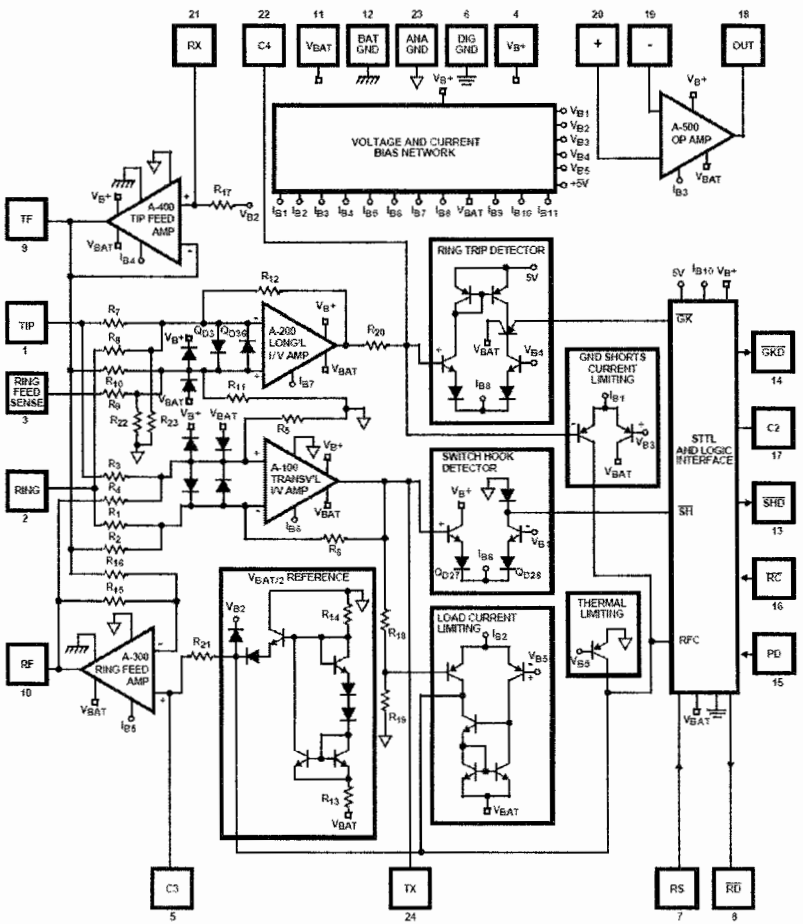
24 PIN SOIC	SYMBOL	DESCRIPTION
21	RX	Receive Input, 4-Wire Side - A high impedance analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the Tip feed and Ring feed terminals, which in turn drive tip and ring through 300Ω of feed resistance on each side of the line.
22	C_4	Capacitor #4 - An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from near by power lines and other noise sources. This capacitor is also required for the proper operation of ring trip detection. Typical value is 0.5µF, to 1.0µF, 20V. This capacitor should be nonpolarized.
23	AG (Note 5)	Analog Ground - To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.
24	TX	Transmit Output, 4-Wire Side - A low impedance analog output which represents the differential voltage across Tip and Ring. Transhybrid balancing must be performed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.
	NC	No internal connection.

Functional Diagram



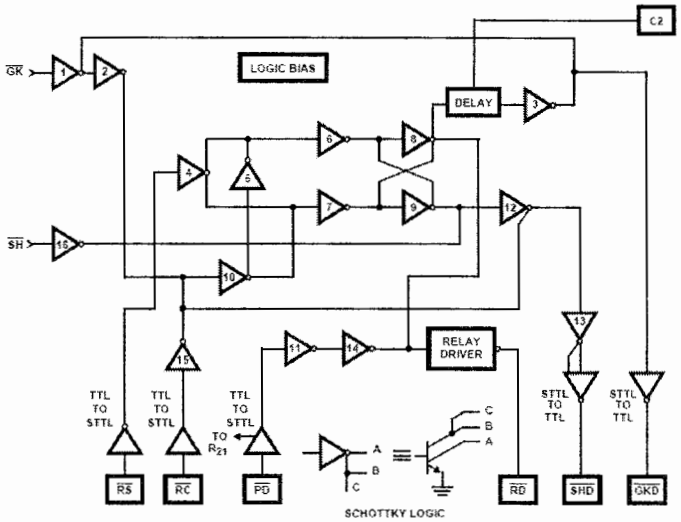
Schematic Diagram

SLIC FUNCTIONAL SCHEMATIC
Pin Numbers for SOIC Package



Schematic Diagram (Continued)

LOGIC GATE SCHEMATIC



Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum of 30mA$_{RMS}$, 15mA$_{RMS}$ per leg, without any performance degradation.

TABLE 1.

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
		±500 (Ceramic)	V_{PEAK}
Metallic Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
		±500 (Ceramic)	V_{PEAK}
T/GND R/GND	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
		±500 (Ceramic)	V_{PEAK}
50/60Hz Current T/GND R/GND	11 Cycles Limited to 10A$_{RMS}$	700 (Plastic)	V_{RMS}
		350 (Ceramic)	V_{RMS}

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

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Applications Diagram

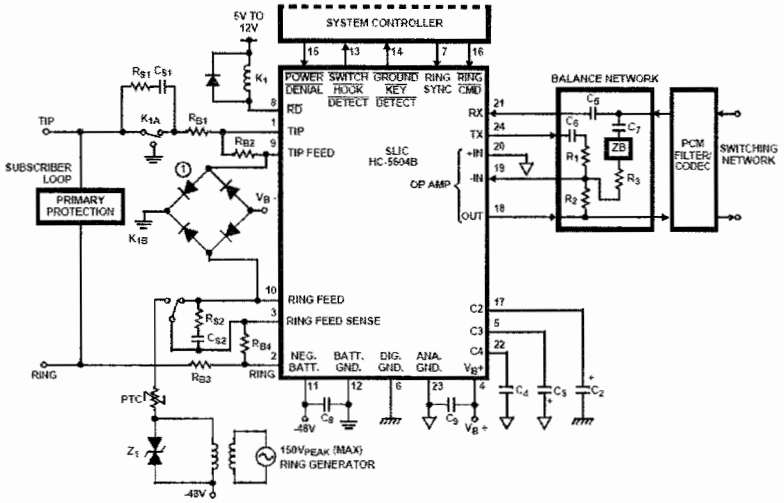


FIGURE 1. TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC

Typical Component Values

C_2 = 0.15µF, 10V.

C_3 = 0.3µF, 30V.

C_4 = 0.5µF to 1.0µF, 10%, 20V (Should be nonpolarized).

C_5 = 0.5µF, 20V.

C_6 = C_7 = 0.5µF (10% Match Required) (Note 7).

C_8 = 0.01µF, 100V.

C_9 = 0.01µF, 20V, ±20%.

R_1 = R_2 = R_3 = 100kΩ (0.1% Match Required, 1% absolute value) $\overline{ZB}$ = 0 for 600Ω Terminations (Note 7).

R_{B1} = R_{B2} = R_{B3} = R_{B4} = 150Ω (0.1% Match Required, 1% absolute value).

R_{S1} = R_{S2} =1kΩ, typically.

C_{S1} = C_{S2} = 0.1µF, 200V typically, depending on V_{RING} and line length.

Z_1 = 150V to 200V transient protection.

PTC used as ring generator ballast.

NOTES:

5. Secondary protection diode bridge recommended is a 2A, 200V type.
6. To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C_6-R_1 and R_2 and C_7-ZB-R_3, to match in impedance to within 0.3%. Thus, if C_6 and C_7 are 1µF each, a 20% match is adequate. It should be noted that the transmit output to C_8 sees a -22V step when the loop is closed. Too large a value for C_8 may produce an excessively long transient at the op amp output to the PCM Filter/CODEC.
   A 0.5µF and 100kΩ gives a time constant of 50ms. The uncommitted op amp output is internally clamped to stay within ±6.6V and is current limited.
7. All grounds (AG, BG, and DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.
8. Application shows Ring Injected Ringing. Balanced or Tip injected configuration may be used.
9. Pin numbers given for SOIC package.

1 Overview

The SICOFI®4-µC is a programmable DSP-based four-channel codec filter device to fulfill worldwide voice telephony standards. An easy to use serial microcontroller interface provides access to 288 bytes of Coefficient RAM (CRAM) and to 32 registers. The values stored in the CRAM determine the filter characteristics of the embedded DSP. Writing to the registers allows control of features such as mode settings, enabling and disabling of filters, tone generators, and test loops, PCM data rates, and signaling and clock output control. Reading from the registers provides status information about the signaling inputs and level metering results.

This document provides detailed information on filter coefficient programming, register configuration settings, and the programming interface. The PEB 2466 is available for standard temperature range applications (0 °C to +70 °C); the PEF 2466 is available for extended temperature range applications (-40 °C to +85 °C).

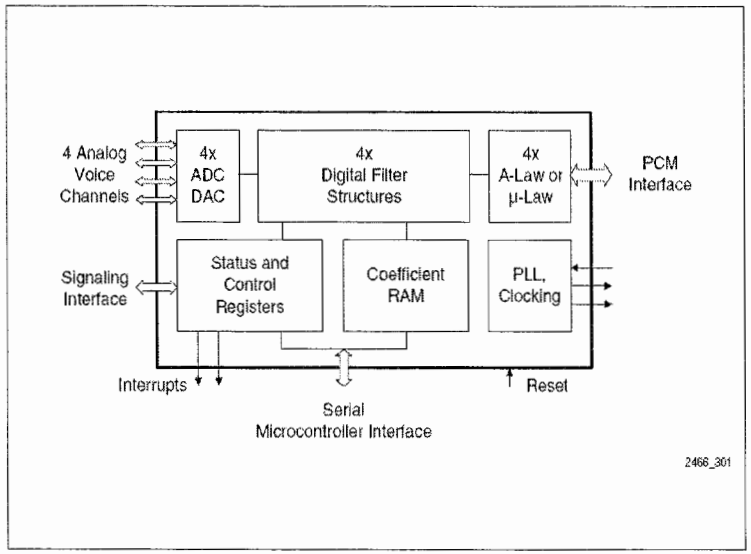


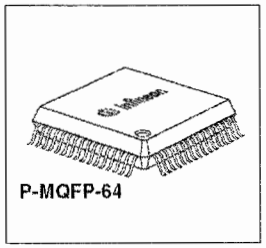
Figure 1 Programmable Four Channel Codec Filter

Four Channel Codec Filter with PCM and Microcontroller Interface
SICOFI®4-µC

PEB 2466
PEF 2466

Version 2.2 **CMOS**

1.1 Features



- Four-channel single chip codec and filter fulfills the ITU-T Q.552, G.712, and all country-specific requirements
- High analog driving capability (300 Ω, 50 pF) for direct driving of transformers
- Digital Signal Processing (DSP) technique
- Programmable digital filters to adapt transmission behavior, especially for:
  - AC impedance matching
  - Transhybrid balancing
  - Frequency response
  - Gain
  - A/µ-Law compression and expansion
- High performance ADC and DAC for excellent linearity and dynamic gain
- Programmable Analog Interface to electronic SLICs or transformer solutions
- Seven SLIC-signaling I/O pins per channel with programmable debouncing
- Two PCM Highways accessible by on-chip PCM Interface
- Programmable time slot assignment and variable data rates from 128 kbit/s to 8 Mbit/s
- Easy to use 4-pin Serial Microcontroller Interface for (SPI compatible) read/write access
- Single supply voltage (5 V)
- Advanced low-power mixed-signal CMOS technology
- Two programmable tone generators per channel (DTMF possible)
- Level metering function for system tests and for analog input signal testing
- Advanced on-chip functions for device and system diagnostics and manufacturing test
  - Five digital loops
  - Four analog loops
- Support tools include:
  - Hardware development board — STUT 2466
  - QSICOS Coefficient Calculation and Register Configuration Software
- Standard P-MQFP-64 package

Type	Package
PEB 2466 Version 2.2	P-MQFP-64
PEF 2466 Version 2.2	P-MQFP-64

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1.2 Logic Symbol

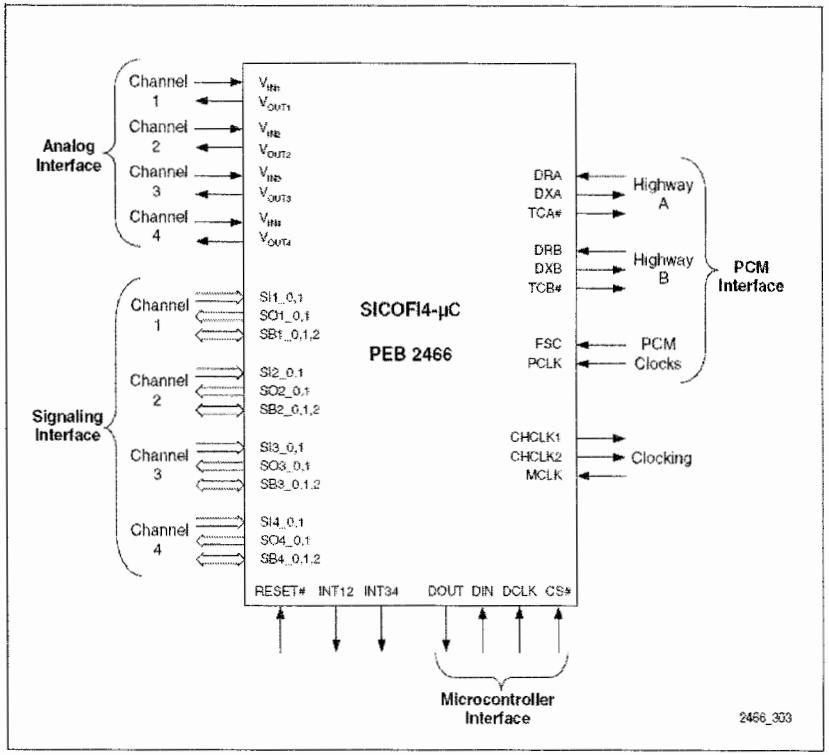

Figure 2 SICOFI®4-µC Logic Symbol

2 Pin Descriptions

2.1 Pin Diagram

(top view)

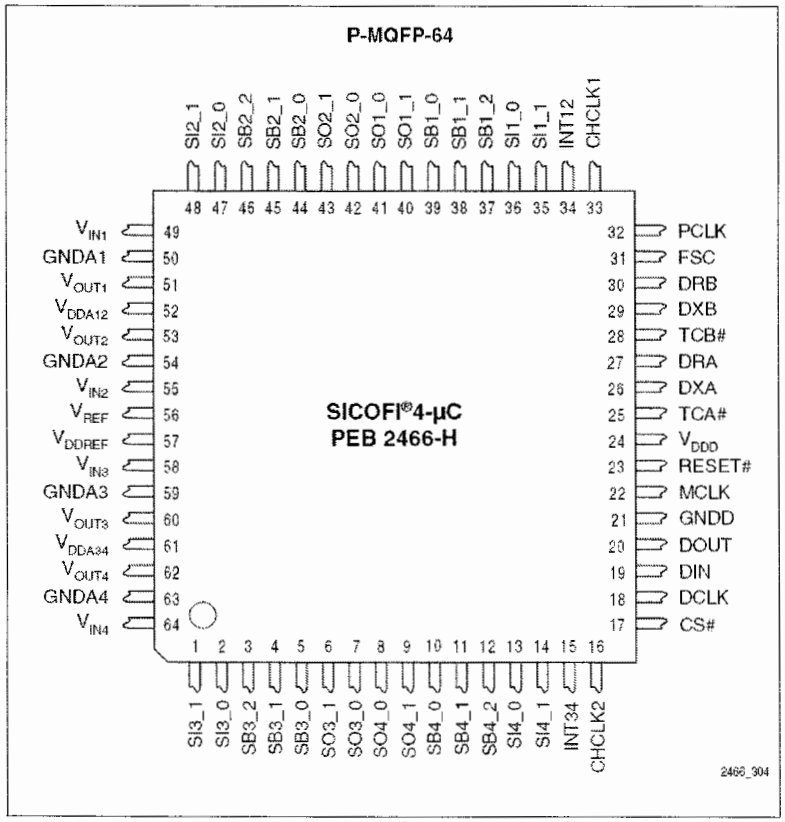

Figure 3 Pin Configuration of SICOFI®4-µC

2.2 Pin Definitions and Functions

Table 1 Pin Definitions and Functions

Pin	Symbol	Type	Function 2466	Ch.
1	SI3_1	I	**Signaling Input, Channel 3 Pin 1** Read logic status from Register Bit XR0.5.	3
2	SI3_0	I	**Signaling Input, Channel 3 Pin 0** Read logic status from Register Bit XR0.4.	3
3	SB3_2	I/O	**Bi-directional Signaling, Channel 3 Pin 2** Set direction in XR3.2, read/write value from/to Bit XR3.6.	3
4	SB3_1	I/O	**Bi-directional Signaling, Channel 3 Pin 1** Set direction in XR2.5, read/write value from/to Bit XR1.5.	3
5	SB3_0	I/O	**Bi-directional Signaling, Channel 3 Pin 0** Set direction in XR2.4, read/write value from/to Bit XR1.4.	3
6	SO3_1	O	**Signaling Output, Channel 3 Pin 1** Write output value to Register Bit XR0.5.	3
7	SO3_0	O	**Signaling Output, Channel 3 Pin 0** Write output value to Register Bit XR0.4.	3
8	SO4_0	O	**Signaling Output, Channel 4 Pin 0** Write output value to Register Bit XR0.6.	4
9	SO4_1	O	**Signaling Output, Channel 4 Pin 1** Write output value to Register Bit XR0.7.	4
10	SB4_0	I/O	**Bi-directional Signaling, Channel 4 Pin 0** Set direction in XR2.6, read/write value from/to Bit XR1.6.	4
11	SB4_1	I/O	**Bi-directional Signaling, Channel 4 Pin 1** Set direction in XR2.7, read/write value from/to Bit XR1.7.	4
12	SB4_2	I/O	**Bi-directional Signaling, Channel 4 Pin 2** Set direction in XR3.3, read/write value from/to Bit XR3.7.	4
13	SI4_0	I	**Signaling Input, Channel 4 Pin 0** Read logic status from Register Bit XR0.6.	4
14	SI4_1	I	**Signaling Input, Channel 4 Pin 1** Read logic status from Register Bit XR0.7.	4
15	INT34	O	**Interrupt Output Channels 3 and 4** Active high.	3,4

Pin	Symbol	Type	Function 2466	Ch.
16	CHCLK2	O	**Chopper Clock Output 2** Provides 256, 512, or 16384 kHz signal; sync. to MCLK. Configured with Register Bits XR5.2 and XR5.3.	all
17	CS#	I	**Chip Select** Microcontroller Interface chip select, enable to read or write; active low.	all
18	DCLK	I	**Data Clock** Microcontroller Interface data clock, shifts data from or to device; maximum clock rate 8192 kHz.	all
19	DIN	I	**Data Input** Microcontroller Interface control data input pin; DCLK determines data rate.	all
20	DOUT	O	**Data Output** Microcontroller Interface control data output pin; DCLK determines data rate: DOUT is high impedance "Z" if no data is transmitted from the SICOFI®4-µC.	all
21	GNDD	I	**Digital Ground** Not internally connected to GNDA1,2,3,4. All digital signals are referred to this pin.	all
22	MCLK	I	**Master Clock Input** Requires a 1536, 2048, 4096 or 8192 kHz signal, sync. to FSC. Select frequency in Register Bits XR5.6 and XR5.7.	all
23	RESET#	I	**Reset Input** Forces the device into default mode; active low.	all
24	V_{DDD}	I	**Digital Supply Voltage** +5 V supply for digital circuits (100 nF blocking cap. required).	all
25	TCA#	O	**Transmit Control Output A** PCM Interface: active if data is transmitted via DXA; active low, open drain.	all
26	DXA	O	**Data Transmit to PCM-Highway A** PCM Interface: PCM data for each channel is transmitted in 8-bit bursts every 125 µs.	all
27	DRA	I	**Data Receive from PCM-Highway A** PCM Interface: PCM data for each channel is received in 8-bit bursts every 125 µs.	all

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Pin Descriptions

Pin	Symbol	Type	Function 2466	Ch.
28	TCB#	O	**Transmit Control Output B** PCM Interface: active if data is transmitted via DXB; active low, open drain.	all
29	DXB	O	**Data Transmit to PCM-highway B** PCM Interface: data for each channel is transmitted in 8-bit bursts every 125 µs.	all
30	DRB	I	**Data Receive from PCM-highway B** PCM Interface: data for each channel is received in 8-bit bursts every 125 µs.	all
31	FSC	I	**Frame Synchronization Clock** 8 kHz; identifies beginning of frame, individual time slots referenced to FSC; FSC must be synchronous to PCLK.	all
32	PCLK	I	**PCM Data Clock** 128 to 8192 kHz; determines the rate at which PCM data is shifted into or out of the PCM-ports.	all
33	CHCLK1	O	**Chopper Clock Output 1** Configurable output clock (T = 2 ... 28 ms), sync. to MCLK. Programmed in Register Bits XR4.0 to XR4.3.	all
34	INT12	O	**Interrupt Output, Channels 1 and 2** Active high.	1,2
35	SI1_1	I	**Signaling Input Channel 1, Pin 1** Read logic status from Register Bit XR0.1.	1
36	SI1_0	I	**Signaling Input Channel 1, Pin 0** Read logic status from Register Bit XR0.0.	1
37	SB1_2	I/O	**Bi-directional Signaling, Channel 1 Pin 2** Set direction in XR3.0, read/write value from/to Bit XR3.4.	1
38	SB1_1	I/O	**Bi-directional Signaling, Channel 1 Pin 1** Set direction in XR2.1, read/write value from/to Bit XR1.1.	1
39	SB1_0	I/O	**Bi-directional Signaling, Channel 1 Pin 0** Set direction in XR2.0, read/write value from/to Bit XR1.0.	1
40	SO1_1	O	**Signaling Output, Channel 1, Pin 1** Write output value to Register Bit XR0.1.	1
41	SO1_0	O	**Signaling Output, Channel 1, Pin 0** Write output value to Register Bit XR0.0.	1
42	SO2_0	O	**Signaling Output, Channel 2, Pin 0** Write output value to Register Bit XR0.2.	2

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Pin	Symbol	Type	Function 2466	Ch.
43	SO2_1	O	**Signaling Output, Channel 2, Pin 1** Write output value to Register Bit XR0.3.	2
44	SB2_0	I/O	**Bi-directional Signaling, Channel 2 Pin 0** Set direction in XR2.2, read/write value from/to Bit XR1.2.	2
45	SB2_1	I/O	**Bi-directional Signaling, Channel 2 Pin 1** Set direction in XR2.3, read/write value from/to Bit XR1.3.	2
46	SB2_2	I/O	**Bi-directional Signaling, Channel 2 Pin 2** Set direction in XR3.1, read/write value from/to Bit XR3.5.	2
47	SI2_0	I	**Signaling Input, Channel 2, Pin 0** Read logic status from Register Bit XR0.2.	2
48	SI2_1	I	**Signaling Input, Channel 2, Pin 1** Read logic status from Register Bit XR0.3.	2
49	V_{IN1}	I	**Analog Voice (Voltage) Input, Channel 1** Requires a coupling capacitor >39 nF to the SLIC.	1
50	GNDA1	I	**Analog Ground, Channel 1** Not internally connected to GNDD or GNDA2,3,4.	1
51	V_{OUT1}	O	**Analog Voice (Voltage) Output, Channel 1** Requires a coupling capacitor to the SLIC. The capacitor value depends on the SLIC's input impedance.	1
52	V_{DDA12}	I	**Analog Supply Voltage, Channels 1 and 2** +5 V (100 nF blocking capacitor required).	1,2
53	V_{OUT2}	O	**Analog Voice (Voltage) Output, Channel 2** Requires a coupling capacitor to the SLIC. The capacitor value depends on the SLIC's input impedance.	2
54	GNDA2	I	**Analog Ground, Channel 2** Not internally connected to GNDD or GNDA 1,3,4.	2
55	V_{IN2}	I	**Analog Voice (Voltage) Input, Channel 2** Requires a coupling capacitor >39 nF to the SLIC.	2
56	V_{REF}	I/O	**Reference Voltage** Must connect to a 220 nF cap. to ground.	all
57	V_{DDREF}	I	**Analog Supply Reference Voltage** +5 V (100 nF blocking capacitor required).	all
58	V_{IN3}	I	**Analog Voice (Voltage) Input, Channel 3** Requires a coupling capacitor >39 nF to the SLIC.	3

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Pin Descriptions

Pin	Symbol	Type	Function 2466	Ch.
59	GNDA3	I	**Analog Ground, Channel 3** Not internally connected to GNDD or GNDA1,2,4.	3
60	V_{OUT3}	O	**Analog Voice (Voltage) Output, Channel 3** Requires a coupling capacitor to the SLIC. The capacitor value depends on the SLIC's input impedance.	3
61	V_{DDA34}	I	**Analog Supply Voltage, Channels 3 and 4** +5 V (100 nF blocking capacitor required).	3,4
62	V_{OUT4}	O	**Analog Voice (Voltage) Output, Channel 4** Requires a coupling capacitor to the SLIC. The capacitor value depends on the SLIC's input impedance.	4
63	GNDA4	I	**Analog Ground, Channel 4** Not internally connected to GNDD or GNDA1,2,3.	4
64	V_{IN4}	I	**Analog Voice (Voltage) Input, Channel 4** Requires a coupling capacitor >39 nF to the SLIC.	4

3 Functional Description

The general architecture of the PEB 2466 is discussed in the ***Product Overview*, Chapter 2**. This *Programmer's Reference Manual* describes the signal processing functions performed by the PEB 2466 and provides detailed information on those blocks and features that are programmable to meet country-specific telephone line requirements, and to adapt to the system environment:

- Analog Amplification/Attenuation,
- Impedance Matching,
- Transhybrid Balancing,
- Digital Amplification/Attenuation,
- Frequency Response Correction,
- Programmable A- or µ-Law Companding.
- Level Metering Functions,
- Two Tone Generators,
- 28 Programmable Input and Output Signals (Signaling Interface),
- Programmable Data Rate of PCM Highway.
- Programmable Time Slots for PCM Highway,
- 4 Analog and 5 Digital Configurable Test Loops, and
- Programmable Clock Outputs.

3.1 Functional Blocks

Based on an advanced digital filter concept, the PEB 2466 provides excellent transmission performance and high flexibility. The PEB 2466 includes both Fixed Blocks and Programmable Blocks. The new filter concept maximizes independence of the different filter blocks. The blocks are illustrated in **Figure 4**.

3.1.1 Fixed Blocks

The fixed blocks (IMFIX1, IMFIX2, XFIX1, XFIX2, RFIX1, RFIX2 and THFIX) describe the transfer functions of the non-programmable blocks of the SICOFI®4-µC.

The fixed blocks in the transmit path (XFIX1 and XFIX2) include the transfer functions of the anti-aliasing prefilter, digital hardware filter, and decimation units.

The fixed blocks in the receive path (RFIX1 and RFIX2) include the transfer functions of the post filter, digital hardware filters, and interpolation blocks. The digital hardware filters are fast, hardwired logic circuits which reduce the amount of data and thus the workload of the DSP. IMFIX1, IMFIX2, and THFIX include functions like fixed delays, interpolation, and decimation blocks for the IM and TH filters.

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Functional Description

3.1.2 Programmable Blocks

The following paragraphs characterize the programmable filter blocks, including the numbers of bits used for programming each filter. These bits must be stored in the SICOFI®4-µC Coefficient RAM. A utility program (QSICOS) is available for calculation and optimization of the coefficients. QSICOS is described and discussed in **Chapter 7** "Application Hints" on page 58.

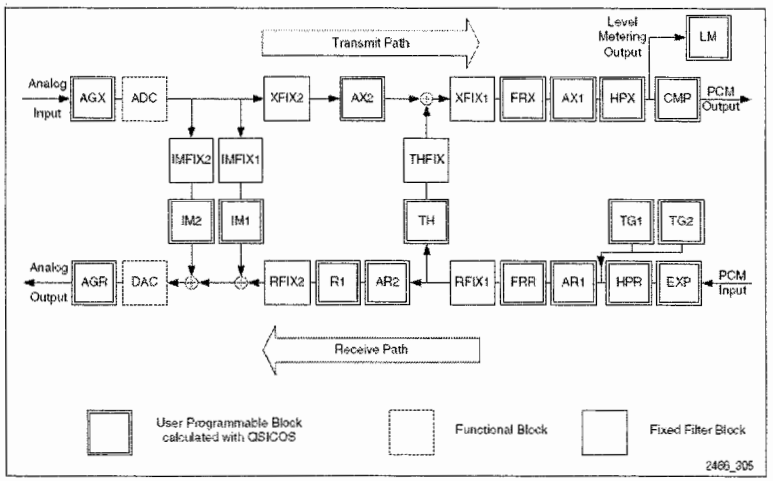

Figure 4 SICOFI®4-µC Detailed Flow Diagram

Analog Amplification/Attenuation (AGX, AGR) Block

In the transmit direction, an amplification of 6.02 dB can be enabled or disabled (CR2.2). In the receive direction, an attenuation of 6.02 dB can be enabled or disabled (CR2.3).

Impedance Matching (IM) Filter

The Impedance Matching (IM) Filters can achieve a return loss better than 30 dB. They consist of 3 different loops: IM2 and the IIR and FIR filters internal to IM1.

The IM2 block works at a sampling rate of 4 MHz and is implemented with a fixed and a programmable element. 12 bits are needed for programming IM2.

The programmable IM1 block has two filter blocks internally which work in parallel: A Wave Digital Filter at 128 kHz for improved low frequency response, and a Finite Impulse Response Filter (FIR) at 64kHz for fine tuning. The Wave Digital Filter is programmed

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with 60 bits. It is an Infinite Impulse Response Filter (IIR) with guaranteed passive behavior and excellent stability. The FIR Filter is programmed with 48 bits.

The real part of the termination impedance is positive under all conditions. The filters also show an improved overflow performance for transients.

When the channel is in operating mode the IM Filters have to be enabled by setting bit CR0.6 to "1" (see **Chapter 6.3.1**). The IM filter coefficients are programmed with the COP_4 and COP_5 command (see **Chapter 6.5** for details). These command sequences also contain the coefficients for the R1 block.

Transhybrid Balancing (TH) Filter

The flexible implementation of the Transhybrid Balancing (TH) Filter allows optimization over a wide impedance range. The resulting Transhybrid Loss can achieve 30 dB (typically better than 40 dB; PEB/PEF 2466 without connecting a SLIC).

The programmable block TH is internally implemented by two filter blocks that work in parallel: A second order Wave Digital Filter (IIR) and a 7-tap FIR Filter. The Wave Digital Filter improves the low frequency response. It is programmed with 106 bits. The 7-tap FIR Filter is programmed with 7*3 nibbles (84 bits) and is used for fine tuning. Both filter blocks work at a sampling frequency of 16 kHz.

The coefficients for the TH Filters are programmed with the COP_0, COP_1 and COP_2 commands (see **Chapter 6.5** for details). For easy adaptation to different lines, four independent coefficient sets can be stored in the CRAM. The TH Filter behavior can be changed quickly by selecting any of the four sets with the bits CR0.0 and CR0.1. Bit CR0.7 enables/disables the TH path.

Frequency Response Correction (FRR and FRX) Filters

Frequency Response Correction (FRR and FRX) Filters are provided for line equalization and compensation of attenuation distortion. The use of minimum phase filters instead of linear phase filters improves the Group Delay Distortions. The Frequency Response Receive (FRR) Filter corrects distortions of the receive path, the Frequency Response Transmit (FRX) Filter performs the same function in transmit direction. Both are implemented as 5-tap programmable FIR filters operating at 8 kHz. Each of them is programmed with 5*3 nibbles (60 bits). Their frequency response is better than 0.1 dB. FRX and FRR coefficients are programmed with the COP_6 and COP_7 commands (see **Chapter 6.5**). Bit CR0.5 enables/disables FRX, Bit CR0.4 enables/disables FRR.

The R1 Filter is also used to compensate the frequency response in the receive path. The programming bits for the R1 Filter are part of the programming sequence for the Impedance Matching Filters (COP_4, COP_5).

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Functional Description

Amplification/Attenuation Filters (AX1, AX2, AR1, AR2)

There are two separate filters in the transmit path and in the receive path, improving the level adjustment in both directions. These blocks allow optimal adjustment of the digital dynamic range. They further improve the transhybrid balancing results and allow gain adjustments independent of the TH Filters.

The Amplification/Attenuation Filters AX1 and AR1 are programmed with 5 nibbles each (20 bits each). The AX2 and AR2 Filters use 3 nibbles (12 bits) each for programming. This results in 32-bit programming information for the AX1 and AX2, and the same number of bits for the AR1 and AR2 filters. As shown below, the granularity of the gain adjustments is very fine.

- Amplification/Attenuation Receive (AR1, AR2) Filter

Range	Step Size
+3 dB to -14 dB	0.02 to 0.05 dB
-14 dB to -24 dB	0.05 dB

- Amplification/Attenuation Transmit (AX1, AX2) Filter

Range	Step Size
-3 dB to +14 dB	0.02 to 0.05 dB
+14 dB to +24 dB	0.05 dB

The coefficients for AX1/AX2 and AR1/AR2 are programmed with the COP_8 and COP_9 commands (see **Chapter 6.5**). Bit CR0.3 enables/disables AX1 and AX2, CR0.2 enables/disables AR1 and AR2.

Total Range for Amplification/Attenuation

The amplification/attenuation of the transmit and receive paths are determined by the accumulated effect of the following blocks:

Attenuation receive: AR = AR1 + FRR + AR2 + R1

Amplification transmit: AX = AX2 + FRX + AX1

The transmission characteristics of the SICOFI®4-µC (see ***Hardware Reference Manual*** **Chapter 4.2**) is guaranteed for the following range of total amplification/ attenuation:

Receive characteristics: -9 dB < AR < 0 dB