DOCUMENTATIONS ANNEXES

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Formulaire

- **Formules de décomposition en série de Fourier :**

Un signal périodique v(t) de période $T = \frac{2\pi}{\omega}$ peut être décomposé sous la forme suivante :

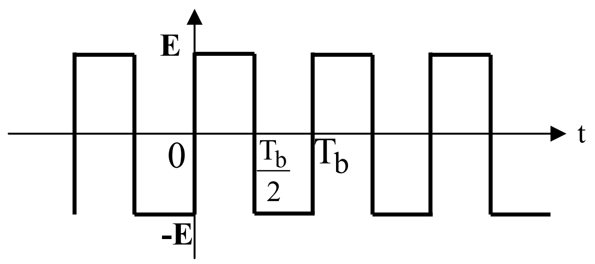
$$v(t) = V_0 + \sum_{n=1}^{+\infty} a_n \cos(n\omega t) + \sum_{n=1}^{+\infty} b_n \sin(n\omega t)$$

$$V_0 = \frac{1}{T}\int_{t_0}^{t_0+T} v(t)dt$$

$$a_n = \frac{2}{T}\int_{t_0}^{t_0+T} v(t)\cos(n\omega t)dt$$

$$b_n = \frac{2}{T}\int_{t_0}^{t_0+T} v(t)\sin(n\omega t)dt$$

- **Décomposition en série de Fourier d'un signal carré :**



$$f(t) = \frac{4E}{\pi}\left[\sin(\omega t) + \frac{1}{3}\sin(3\omega t) + \frac{1}{5}\sin(5\omega t) + ...\right]$$

Syntaxe pour le pseudo-code

Opérateurs

Les opérateurs de calcul sont répartis en 4 groupes de priorité, de la plus forte à la plus faible :

```
@ , ^ , NON
* , / , DIV , MOD , ET , << , >>
+ , - , OU , OUEX
= , <> , < , > , <= , >=
```

Dans une expression, les parenthèses peuvent naturellement être utilisées pour modifier cet ordre de priorité.

Opérateurs arithmétiques

```
+       addition                                      [*]
-       soustraction / changement de signe            [*]
*       multiplication                                [*]
/       division réelle                               [*]
DIV     division entière
MOD     reste de la division entière (modulo)
```

Opérateurs binaires (bit à bit)

```
NON     négation binaire
ET      ET binaire
OU      OU binaire
OUEX    OU Exclusif binaire
<<      décalage à gauche
>>      décalage à droite
```

Opérateurs d'accès

```
=       affectation
@       adresse de (préfixe)                          [*]
^       contenu de (suffixe)                          [*]
[]      accès à un élément de tableau                 [*]
.       accès au champ d'un enregistrement            [*]
^.      accès au champ d'un enregistrement pointé     [*]
->      autre écriture de ^.                          [*]
```

Opérateurs relationnels

```
==      équivalent à                                  [*]
!=      différent de                                  [*]
<       inférieur à                                   [*]
>       supérieur à                                   [*]
<=      inférieur ou égal à                           [*]
>=      supérieur ou égal à                           [*]
```

Opérateurs logiques

```
NON     négation logique
ET      ET logique
OU      OU logique
OUEX    OU Exclusif logique
```

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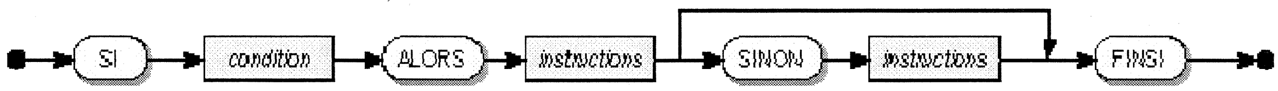
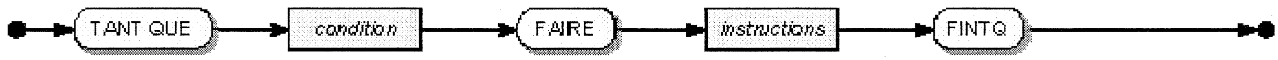
Structures fondamentales

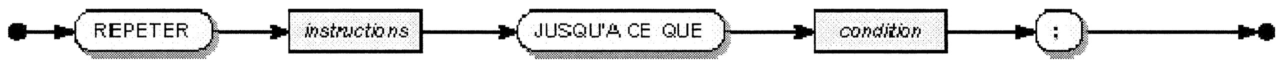
Les structures nécessaires et suffisantes en programmation structurée sont l'alternative, partielle ou complète, et les itérations.



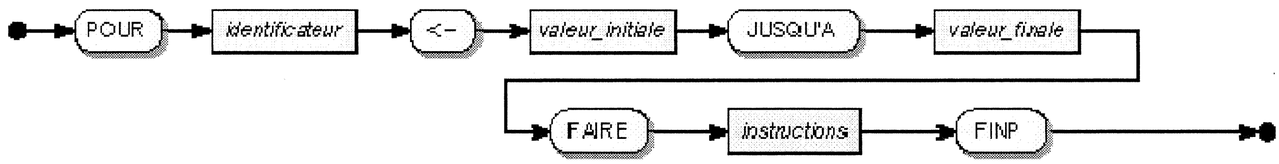
Alternative



Itération à condition initiale



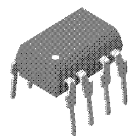
Itération à condition finale

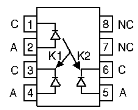


Boucle

Linear Optocoupler, High Gain Stability, Wide Bandwidth

Features
- Couples AC and DC signals
- 0.01 % Servo Linearity
- Wide Bandwidth, > 200 kHz
- High Gain Stability, ± 0.05 %/ °C
- Low Input-Output Capacitance
- Low Power Consumption, < 15 mW
- Isolation Test Voltage, 5300 V_{RMS}, 1.0 sec.
- Internal Insulation Distance, > 0.4 mm for VDE





Agency Approvals
- UL File #E52744
- DIN EN 60747-5-2(VDE0884)
  DIN EN 60747-5-5 pending
  Available with Option 1, Add -X001 Suffix

Applications
Power Supply Feedback Voltage/Current
Medical Sensor Isolation
Audio Signal Interfacing
Isolated Process Control Transducers
Digital Telephone Isolation

Description
The IL300 Linear Optocoupler consists of an AlGaAs IRLED irradiating an isolated feedback and an output PIN photodiode in a bifurcated arrangement. The feedback photodiode captures a percentage of the LED's flux and generates a control signal (I_{P1}) that can be used to servo the LED drive current. This technique compensates for the LED's non-linear, time, and temperature characteristics. The output PIN photodiode produces an output signal (I_{P2}) that is linearly related to the servo optical flux created by the LED.

The time and temperature stability of the input-output coupler gain (K3) is insured by using matched PIN photodiodes that accurately track the output flux of the LED.

Order Information

Part	Remarks
IL300	K3 = 0.557 - 1.618, DIP-8
IL300-DEFG	K3 = 0.765 - 1.181, DIP-8
IL300-EF	K3 = 0.851 - 1.061, DIP-8
IL300-E	K3 = 0.851 - 0.955, DIP-8
IL300-F	K3 = 0.945 - 1.061, DIP-8
IL300-X006	K3 = 0.557 - 1.618, DIP-8 400mil (option 6)
IL300-X007	K3 = 0.557 - 1.618, SMD-8 (option 7)
IL300-X009	K3 = 0.557 - 1.618, SMD-8 (option 9)
IL300-DEFG-X006	K3 = 0.765 - 1.181, DIP-8 400 mil (option 6)
IL300-DEFG-X007	K3 = 0.765 - 1.181, SMD-8 (option 7)
IL300-DEFG-X009	K3 = 0.765 - 1.181, SMD-8 (option 9)
IL300-EF-X006	K3 = 0.851 - 1.061, DIP-8 400 mil (option 6)
IL300-EF-X007	K3 = 0.851 - 1.061, SMD-8 (option 7)
IL300-EF-X009	K3 = 0.851 - 1.061, SMD-8 (option 9)
IL300-E-X006	K3 = 0.851 - 0.955, DIP-8 400 mil (option 6)
IL300-E-X007	K3 = 0.851 - 0.955, SMD-8 (option 7)
IL300-E-X009	K3 = 0.851 - 0.955, SMD-8 (option 9)
IL300-F-X006	K3 = 0.945 - 1.061, DIP-8 400 mil (option 6)
IL300-F-X007	K3 = 0.945 - 1.061, SMD-8 (option 7)
IL300-F-X009	K3 = 0.945 - 1.061, SMD-8 (option 9)

For additional information on the available options refer to Option Information.

Operation Description
A typical application circuit (Figure 1) uses an operational amplifier at the circuit input to drive the LED. The feedback photodiode sources current to R1 connected to the inverting input of U1. The photocurrent, I_{P1}, will be of a magnitude to satisfy the relationship of ($I_{P1} = V_{IN}/R1$).

The magnitude of this current is directly proportional to the feedback transfer gain (K1) times the LED drive current ($V_{IN}/R1 = K1 \bullet I_F$). The op-amp will supply LED current to force sufficient photocurrent to keep the node voltage (Vb) equal to Va.

The output photodiode is connected to a non-inverting voltage follower amplifier. The photodiode load resistor, R2, performs the current to voltage conversion. The output amplifier voltage is the product of the output forward gain (K2) times the LED current and photodiode load, R2 ($V_O = I_F \bullet K2 \bullet R2$).

Therefore, the overall transfer gain (V_O/V_{IN}) becomes the ratio of the product of the output forward gain (K2) times the photodiode load resistor (R2) to the product of the feedback transfer gain (K1) times the input resistor (R1). This reduces to

$V_O/V_{IN}=(K2 \bullet R2)/(K1 \bullet R1)$.

The overall transfer gain is completely independent of the LED forward current. The IL300 transfer gain (K3) is expressed as the ratio of the output gain (K2) to the feedback gain (K1). This shows that the circuit gain becomes the product of the IL300 transfer gain times the ratio of the output to input resistors

$V_O/V_{IN} = K3\ (R2/R1)$.

K1-Servo Gain
The ratio of the input photodiode current (I_{P1}) to the LED current (I_F) i.e., $K1 = I_{P1}/I_F$.

K2-Forward Gain
The ratio of the output photodiode current (I_{P2}) to the LED current (I_F), i.e., $K2 = I_{P2}/I_F$.

K3-Transfer Gain
The Transfer Gain is the ratio of the Forward Gain to the Servo gain, i.e., K3 = K2/K1.

ΔK3-Transfer Gain Linearity
The percent deviation of the Transfer Gain, as a function of LED or temperature from a specific Transfer Gain at a fixed
LED current and temperature.

Photodiode
A silicon diode operating as a current source. The output current is proportional to the incident optical flux supplied by the LED emitter. The diode is operated in the photovoltaic or photoconductive mode. In the photovoltaic mode the diode functions as a current source in parallel with a forward biased silicon diode.

The magnitude of the output current and voltage is dependent upon the load resistor and the incident LED optical flux. When operated in the photoconductive mode the diode is connected to a bias supply which reverse biases the silicon diode. The magnitude of the output current is directly proportional to the LED incident optical flux.

LED (Light Emitting Diode)
An infrared emitter constructed of AlGaAs that emits at 890 nm operates efficiently with drive current from 500 µA to 40 mA. Best linearity can be obtained at drive currents between 5.0 mA to 20 mA. Its output flux typically changes by - 0.5 % /°C over the above operational current range.

Application Circuit

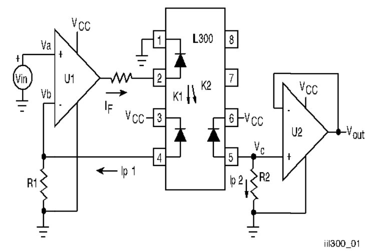


Fig. 1 Typical Application Circuit

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Absolute Maximum Ratings

T_{amb} = 25 °C, unless otherwise specified
Stresses in excess of the absolute Maximum Ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this document. Exposure to absolute Maximum Rating for extended periods of the time can adversely affect reliability.

Input

Parameter	Test condition	Symbol	Value	Unit
Power dissipation		P_{diss}	160	mW
Derate linearly from 25 °C			2.13	mW/°C
Forward current		I_F	60	mA
Surge current (pulse width < 10 µs)		I_{PK}	250	mA
Reverse voltage		V_R	5.0	V
Thermal resistance		R_{th}	470	K/W
Junction temperature		T_j	100	°C

Output

Parameter	Test condition	Symbol	Value	Unit
Power dissipation		P_{diss}	50	mA
Derate linearly from 25 °C			0.65	mW/°C
Reverse voltage		V_R	50	V
Junction temperature		T_j	100	°C
Thermal resistance		R_{th}	1500	K/W

Coupler

Parameter	Test condition	Symbol	Value	Unit
Total package dissipation at 25 °C		P_{tot}	210	mW
Derate linearly from 25 °C			2.8	mW/°C
Storage temperature		T_{stg}	- 55 to + 150	°C
Operating temperature		T_{amb}	- 55 to + 100	°C
Isolation test voltage			> 5300	V_{RMS}
Isolation resistance	V_{IO} = 500 V, T_{amb} = 25 °C	R_{IO}	> 10^{12}	Ω
	V_{IO} = 500 V, T_{amb} = 100 °C	R_{IO}	> 10^{11}	Ω

Electrical Characteristics

T_{amb} = 25 °C, unless otherwise specified
Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluation. Typical values are for information only and are not part of the testing requirements.

Input

LED Emitter

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
Forward voltage	I_F = 10 mA	V_F		1.25	1.50	V
V_F Temperature coefficient		$\Delta V_F/\Delta$ °C		- 2.2		mV/°C
Reverse current	V_R = 5 V	I_R		1.0		µA
Junction capacitance	V_F = 0 V, f = 1.0 MHz	C_j		15		pF
Dynamic resistance	I_F = 10 mA	$\Delta V_F/\Delta I_F$		6.0		Ω

Output

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
Dark current	V_{det} = -15 V, I_F = 0 µs	I_D		1.0	25	nA
Open circuit voltage	I_F = 10 mA	V_D		500		mV
Short circuit current	I_F = 10 mA	I_{SC}		70		µA
Junction capacitance	V_F = 0, f = 1.0 MHz	C_j		12		pF
Noise equivalent power	V_{det} = 15 V	NEP		4×10^{14}		W/√Hz

Coupler

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
Input- output capacitance	V_F = 0 V, f = 1.0 MHz			1.0		pF
K1, Servo gain (I_{P1}/I_F)	I_F = 10 mA, V_{det} = - 15 V	K1	0.0050	0.007	0.011	
Servo current, see Note 1,2	I_F = 10 mA, V_{det} = - 15 V	I_{P1}		70		µA
K2, Forward gain (I_{P2}/I_F)	I_F = 10 mA, V_{det} = - 15 V	K2	0.0036	0.007	0.011	
Forward current	I_F = 10 mA, V_{det} = - 15 V	I_{P2}		70		µA
K3, Transfer gain (K2/K1) see Note 1,2	I_F = 10 mA, V_{det} = - 15 V	K3	0.56	1.00	1.65	K2/K1
Transfer gain linearity	I_F = 1.0 to 10 mA	ΔK3		± 0.25		%
	I_F = 1.0 to 10 mA, T_{amb} = 0 °C to 75 °C			± 0.5		%
Photoconductive Operation						
Frequency response	I_{Fq} = 10 mA, MOD = ± 4.0 mA, R_L = 50 Ω	BW (-3 db)		200		KHz
Phase response at 200 kHz	V_{det} = - 15 V			-45		Deg.

1. Bin Sorting:

K3 (transfer gain) is sorted into bins that are ± 6 % , as follows:

Bin A = 0.557 - 0.626

Bin B = 0.620 - 0.696

Bin C = 0.690 - 0.773

Bin D = 0.765 - 0.859

Bin E = 0.851 - 0.955

Bin F = 0.945 - 1.061

Bin G = 1.051 - 1.181

Bin H = 1.169 - 1.311

Bin I = 1.297 - 1.456

Bin J = 1.442 - 1.618

K3 = K2/K1. K3 is tested at I_F = 10 mA, V_{det} = - 15 V.

2. Bin Categories: All IL300s are sorted into a K3 bin, indicated by an alpha character that is marked on the part. The bins range from "A" through "J".

The IL300 is shipped in tubes of 50 each. Each tube contains only one category of K3. The category of the parts in the tube is marked on the tube label as well as on each individual part.

3. Category Options: Standard IL300 orders will be shipped from the categories that are available at the time of the order. Any of the ten categories may be shipped. For customers requiring a narrower selection of bins, four different bin option parts are offered.

IL300-DEFG: Order this part number to receive categories D,E,F,G only.

IL300-EF: Order this part number to receive categories E, F only.

IL300-E: Order this part number to receive category E only.

Switching Characteristics

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
Switching time	ΔI_F = 2.0 mA, I_{Fq} = 10 mA	t_r		1.0		µs
		t_f		1.0		µs
Rise time		t_r		1.75		µs
Fall time		t_f		1.75		µs

Common Mode Transient Immunity

Parameter	Test condition	Symbol	Min	Typ.	Max	Unit
Common mode capacitance	V_F = 0, f = 1. MHz	C_{CM}		0.5		pF
Common mode rejection ratio	f = 60 Hz, R_L = 2.2 KΩ	CMRR		130		dB

Typical Characteristics (T_{amb} = 25 °C unless otherwise specified)

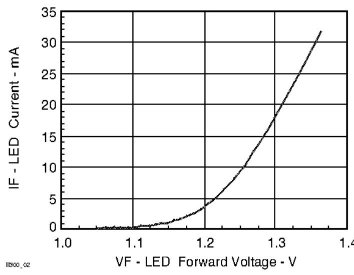

Fig. 2 LED Forward Current vs.Forward Voltage

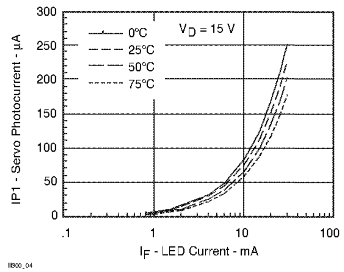

Fig. 4 Servo Photocurrent vs. LED Current and Temperature

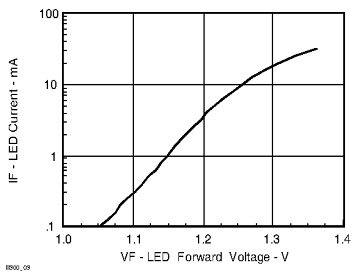

Fig. 3 LED Forward Current vs.Forward Voltage

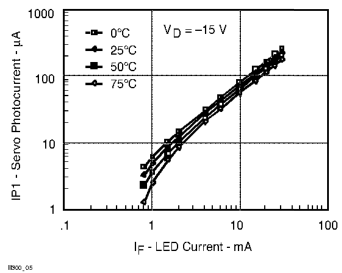

Fig. 5 Servo Photocurrent vs. LED Current and Temperature

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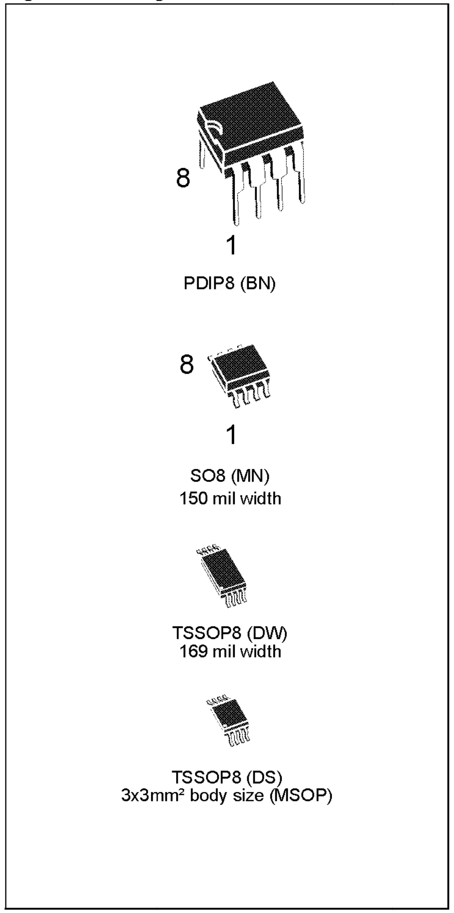
M24C64
M24C32

64Kbit and 32Kbit Serial I²C Bus EEPROM

FEATURES SUMMARY

- Two Wire I²C Serial Interface Supports 400 kHz Protocol
- Single Supply Voltage:
  - 4.5V to 5.5V for M24Cxx
  - 2.5V to 5.5V for M24Cxx-W
  - 1.8V to 5.5V for M24Cxx-R
- Write Control Input
- BYTE and PAGE WRITE (up to 32 Bytes)
- RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Behavior
- More than 1 Million Erase/Write Cycles
- More than 40 Year Data Retention

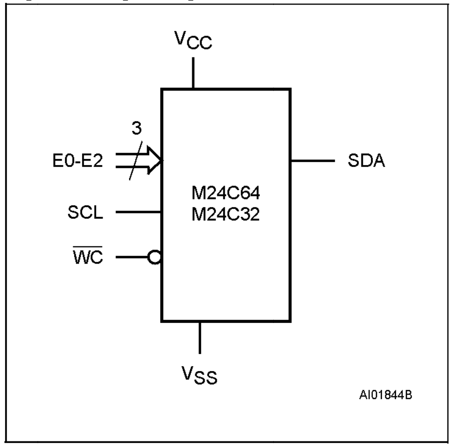
Figure 1. Packages



SUMMARY DESCRIPTION

These I²C-compatible electrically erasable programmable memory (EEPROM) devices are organized as 8192 x 8 bits (M24C64) and 4096 x 8 bits (M24C32).

Figure 2. Logic Diagram



These devices are compatible with the I²C memory protocol. This is a two wire serial interface that uses a bi-directional data bus and serial clock. The devices carry a built-in 4-bit Device Type Identifier code (1010) in accordance with the I²C bus definition.

The device behaves as a slave in the I²C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a Device Select Code and R$\overline{W}$ bit (as described in Table 2), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

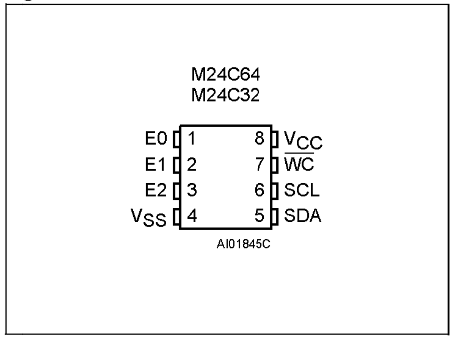
Table 1. Signal Names

E0, E1, E2	Chip Enable
SDA	Serial Data
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Power On Reset: V_{CC} Lock-Out Write Protect

In order to prevent data corruption and inadvertent Write operations during Power-up, a Power On Reset (POR) circuit is included. The internal reset is held active until V_{CC} has reached the POR threshold value, and all operations are disabled – the device will not respond to any command. In the same way, when V_{CC} drops from the operating voltage, below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable and valid V_{CC} must be applied before applying any logic signal.

Figure 3. DIP, SO and TSSOP Connections



Note: 1. See page 18 (onwards) for package dimensions, and how to identify pin-1.

SIGNAL DESCRIPTION

Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor must be connected from Serial Clock (SCL) to V_{CC}. (Figure 4 indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

Serial Data (SDA)

This bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to V_{CC}. (Figure 4 indicates how the value of the pull-up resistor can be calculated).

Chip Enable (E0, E1, E2)

These input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit Device Select Code. These inputs must be tied to V_{CC} or V_{SS}, to establish the Device Select Code.

Write Control ($\overline{WC}$)

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control ($\overline{WC}$) is driven High. When unconnected, the signal is internally read as V_{IL}, and Write operations are allowed.

When Write Control ($\overline{WC}$) is driven High, Device Select and Address bytes are acknowledged, Data bytes are not acknowledged.

Figure 4. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I²C Bus

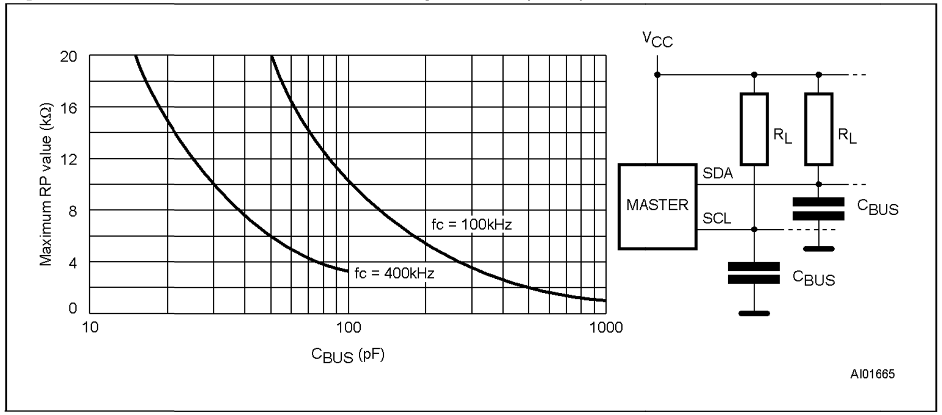


Figure 5. I²C Bus Protocol

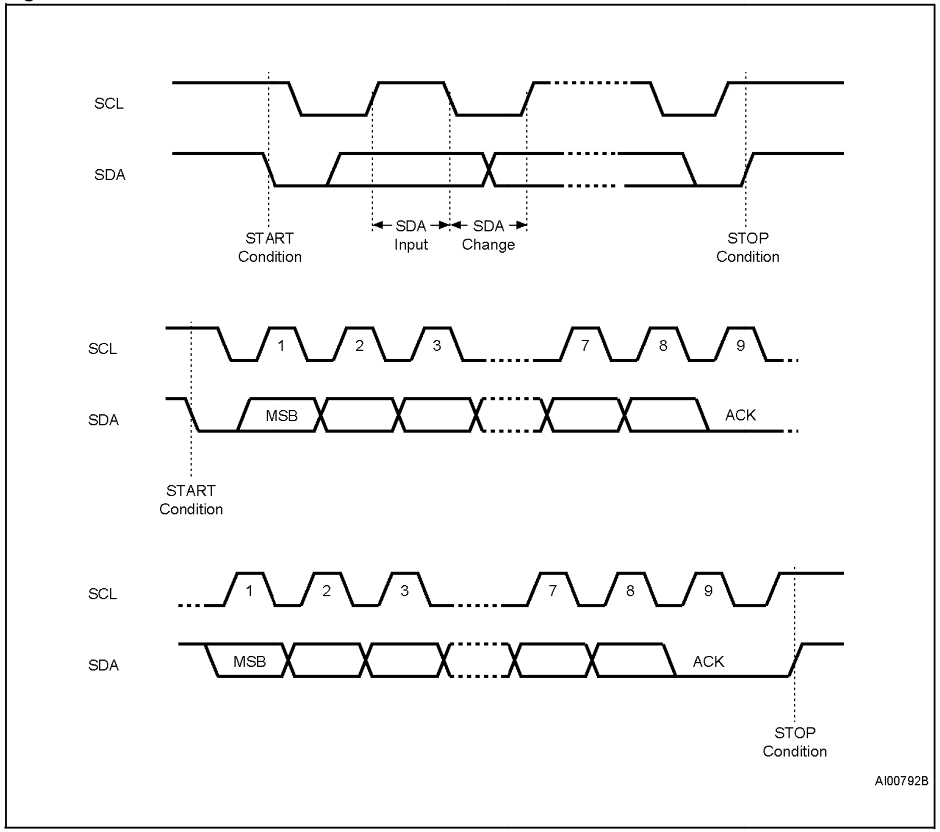


Table 2. Device Select Code

	Device Type Identifier[1]				Chip Enable Address[2]			$R\overline{W}$
	b7	b6	b5	b4	b3	b2	b1	b0
Device Select Code	1	0	1	0	E2	E1	E0	$R\overline{W}$

Note: 1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared against the respective external pins on the memory device.

Table 3. Most Significant Byte

b15	b14	b13	b12	b11	b10	b9	b8

Table 4. Least Significant Byte

b7	b6	b5	b4	b3	b2	b1	b0

Tournez la page S.V.P.

DEVICE OPERATION

The device supports the I²C protocol. This is summarized in Figure 5. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The M24Cxx device is always a slave in all communication.

Start Condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the High state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

Stop Condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven High. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the device into the Stand-by mode. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle.

Acknowledge Bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9^{th} clock pulse period, the receiver pulls Serial Data (SDA) Low to acknowledge the receipt of the eight data bits.

Data Input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven Low.

Memory Addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the Device Select Code, shown in Table 2 (on Serial Data (SDA), most significant bit first).

The Device Select Code consists of a 4-bit Device Type Identifier, and a 3-bit Chip Enable "Address" (E2, E1, E0). To address the memory array, the 4-bit Device Type Identifier is 1010b.

Up to eight memory devices can be connected on a single I²C bus. Each one is given a unique 3-bit code on the Chip Enable (E0, E1, E2) inputs. When the Device Select Code is received on Serial Data (SDA), the device only responds if the Chip Enable Address is the same as the value on the Chip Enable (E0, E1, E2) inputs.

The 8^{th} bit is the Read/$\overline{\text{Write}}$ bit (R$\overline{\text{W}}$). This bit is set to 1 for Read and 0 for Write operations.

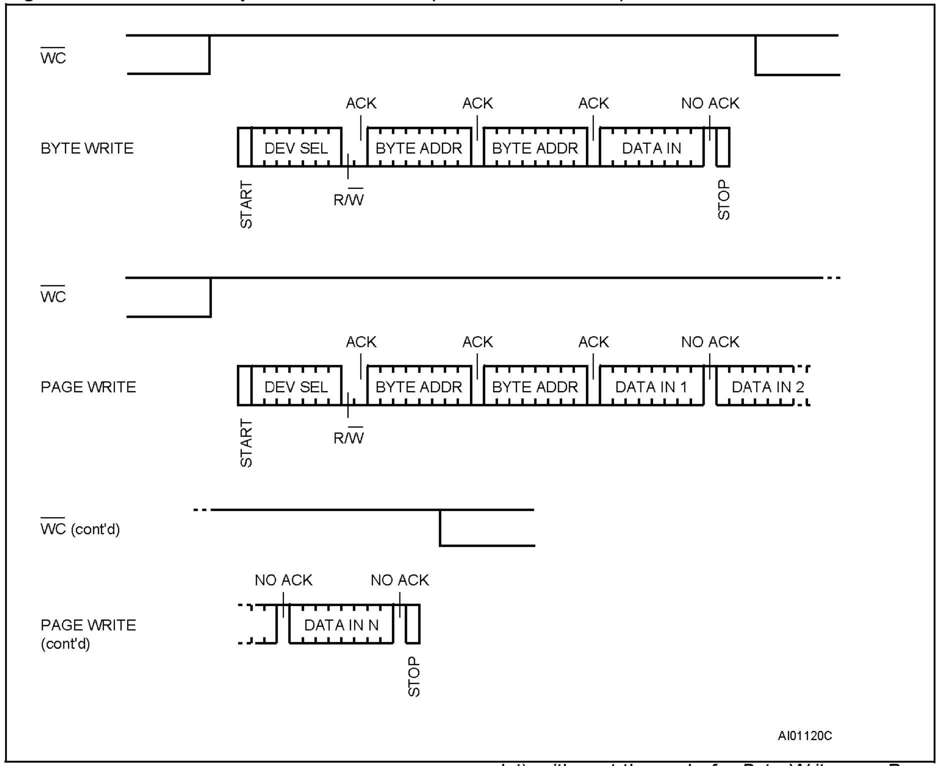
If a match occurs on the Device Select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9^{th} bit time. If the device does not match the Device Select code, it deselects itself from the bus, and goes into Stand-by mode.

Table 5. Operating Modes

Mode	R$\overline{\text{W}}$ bit	$\overline{\text{WC}}$ [1]	Bytes	Initial Sequence
Current Address Read	1	X	1	START, Device Select, R$\overline{\text{W}}$ = 1
Random Address Read	0	X	1	START, Device Select, R$\overline{\text{W}}$ = 0, Address
	1	X		reSTART, Device Select, R$\overline{\text{W}}$ = 1
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	START, Device Select, R$\overline{\text{W}}$ = 0
Page Write	0	V_{IL}	≤ 32	START, Device Select, R$\overline{\text{W}}$ = 0

Note: 1. X = V_{IH} or V_{IL}.

Figure 6. Write Mode Sequences with $\overline{\text{WC}}$=1 (data write inhibited)



Write Operations

Following a Start condition the bus master sends a Device Select Code with the R$\overline{\text{W}}$ bit reset to 0. The device acknowledges this, as shown in Figure 7, and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data byte.

Writing to the memory may be inhibited if Write Control ($\overline{\text{WC}}$) is driven High. Any Write instruction with Write Control ($\overline{\text{WC}}$) driven High (during a period of time from the Start condition until the end of the two address bytes) will not modify the memory contents, and the accompanying data bytes are *not* acknowledged, as shown in Figure 6.

Each data byte in the memory has a 16-bit (two byte wide) address. The Most Significant Byte (Table 3) is sent first, followed by the Least Significant Byte (Table 4). Bits b15 to b0 form the address of the byte in memory.

When the bus master generates a Stop condition immediately after the Ack bit (in the "10^{th} bit" time slot), either at the end of a Byte Write or a Page Write, the internal memory Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

Byte Write

After the Device Select code and the address bytes, the bus master sends one data byte. If the addressed location is Write-protected, by Write Control ($\overline{\text{WC}}$) being driven High, the device replies with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in Figure 7.

Page Write

The Page Write mode allows up to 32 bytes to be written in a single Write cycle, provided that they are all located in the same 'row' in the memory: that is, the most significant memory address bits (b12-b5 for M24C64, and b12-b5 for M24C32) are the same. If more bytes are sent than will fit up to the end of the row, a condition known as 'roll-over' occurs. This should be avoided, as data starts to become overwritten in an implementation dependent way.

The bus master sends from 1 to 32 bytes of data, each of which is acknowledged by the device if Write Control ($\overline{WC}$) is Low. If Write Control ($\overline{WC}$) is High, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck. After each byte is transferred, the internal byte address counter (the 5 least significant address bits only) is incremented. The transfer is terminated by the bus master generating a Stop condition.

Figure 7. Write Mode Sequences with $\overline{WC}$=0 (data write enabled)

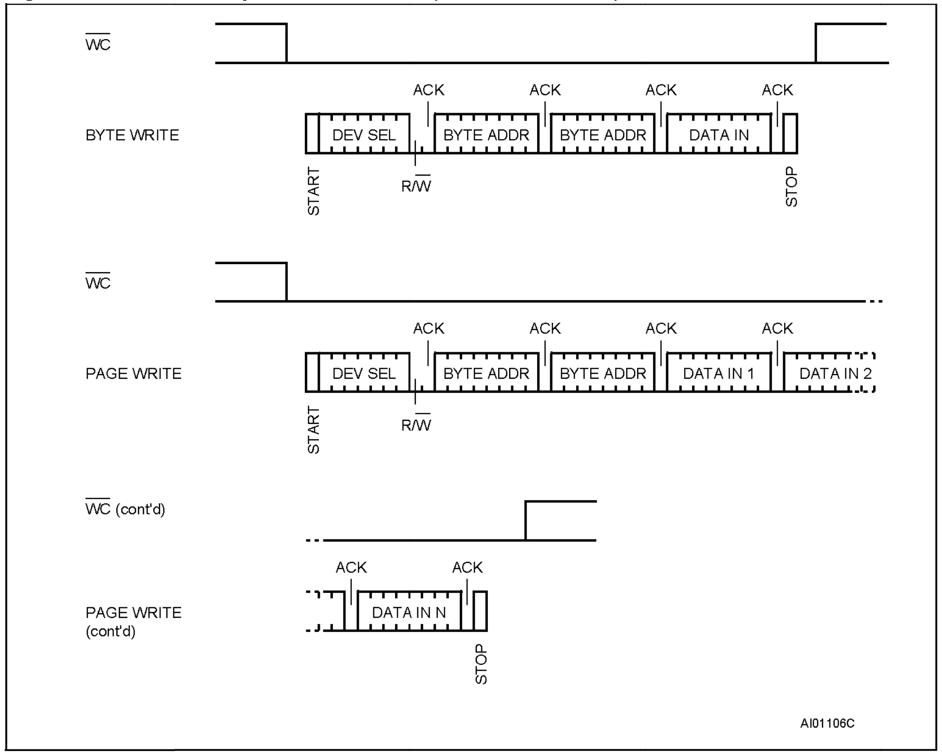
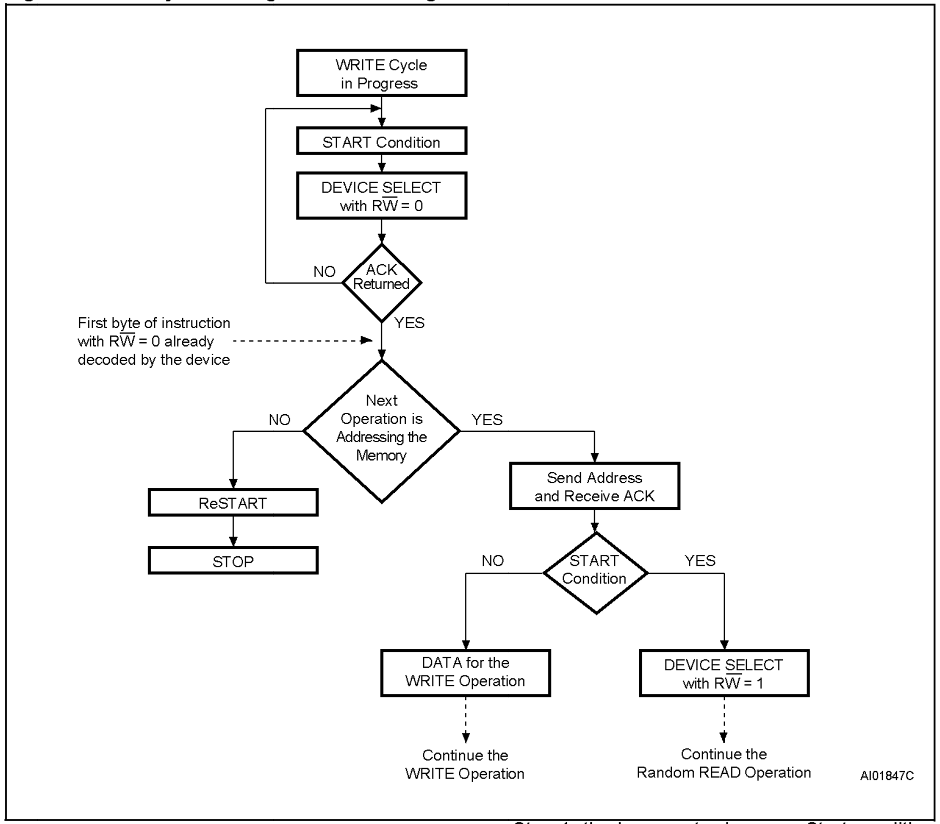


Figure 8. Write Cycle Polling Flowchart using ACK



Minimizing System Delays by Polling On ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_W) is shown in Tables 17 and 18, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in Figure 8, is:

– Initial condition: a Write cycle is in progress.

– Step 1: the bus master issues a Start condition followed by a Device Select Code (the first byte of the new instruction).

– Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

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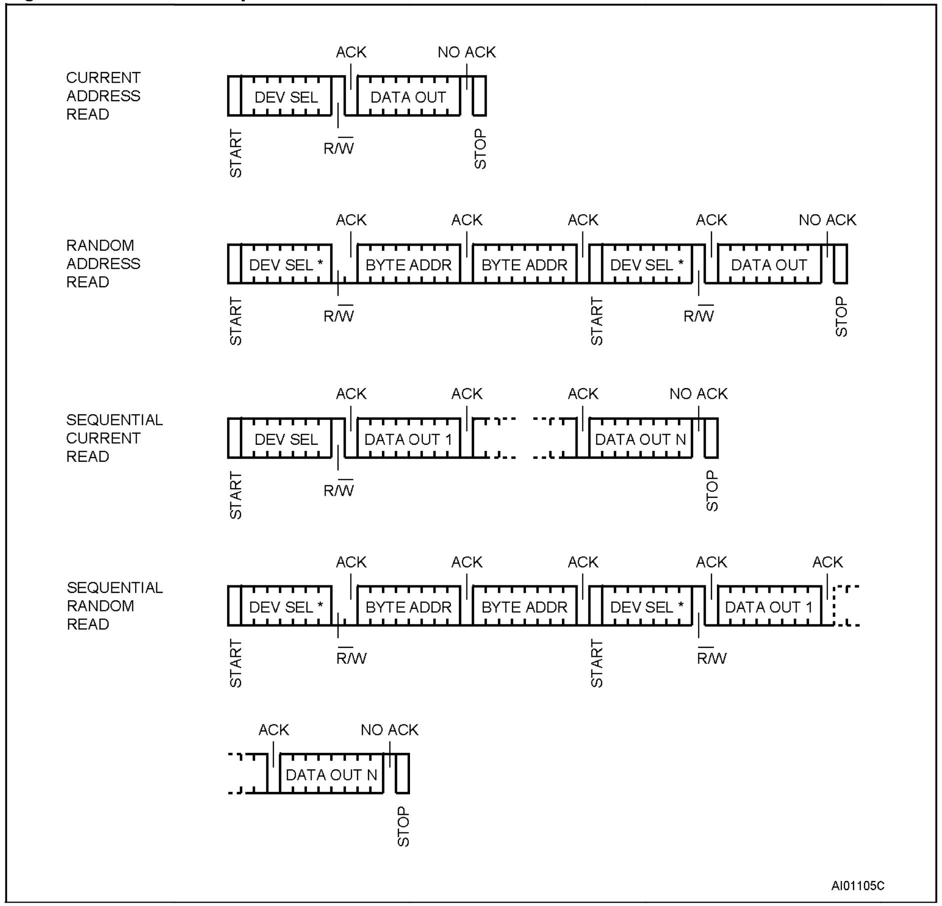
Figure 9. Read Mode Sequences



Note: 1. The seven most significant bits of the Device Select Code of a Random Read (in the 1st and 4th bytes) must be identical.

Read Operations

Read operations are performed independently of the state of the Write Control ($\overline{WC}$) signal.

Random Address Read

A dummy Write is performed to load the address into the address counter (as shown in Figure 9) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the Device Select Code, with the $R\overline{W}$ bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

Current Address Read

The device has an internal address counter which is incremented each time a byte is read. For the Current Address Read operation, following a Start condition, the bus master only sends a Device Select Code with the $R\overline{W}$ bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in Figure 9, *without* acknowledging the byte.

Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus

master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in Figure 9.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 00h.

Acknowledge in Read Mode

For all Read commands, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) Low during this time, the device terminates the data transfer and switches to its Standby mode.

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute Maximum Ratings

Symbol	Parameter		Min.	Max.	Unit
T_{STG}	Storage Temperature		–65	150	°C
T_{LEAD}	Lead Temperature during Soldering	PDIP: 10 seconds SO: 20 seconds (max) [1] TSSOP: 20 seconds (max) [1]		260 235 235	°C
V_{IO}	Input or Output range		–0.6	6.5	V
V_{CC}	Supply Voltage		–0.3	6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]		–4000	4000	V

Note: 1. IPC/JEDEC J-STD-020A
2. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 7. Operating Conditions (M24Cxx)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
T_A	Ambient Operating Temperature	–40	85	°C

Table 8. Operating Conditions (M24Cxx-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.5	5.5	V
T_A	Ambient Operating Temperature	–40	85	°C

Table 9. Operating Conditions (M24Cxx-R)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	1.8	5.5	V
T_A	Ambient Operating Temperature	–40	85	°C

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Table 10. AC Measurement Conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	100		pF
	Input Rise and Fall Times		50	ns
	Input Levels	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input and Output Timing Reference Levels	$0.3V_{CC}$ to $0.7V_{CC}$		V

Figure 10. AC Measurement I/O Waveform

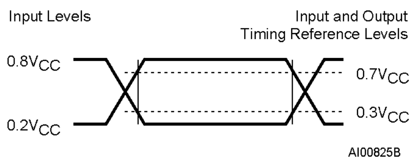

Table 11. Input Parameters

Symbol	Parameter[1,2]	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} < 0.5$ V	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} > 0.7V_{CC}$	500		kΩ
t_{NS}	Pulse width ignored (Input Filter on SCL and SDA)	Single glitch		100	ns

Note: 1. $T_A = 25$ °C, f = 400 kHz
2. Sampled only, not 100% tested.

Table 12. DC Characteristics (M24Cxx)

Symbol	Parameter	Test Condition (in addition to those in Table 7)	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA, E2, E1, E0)	$V_{IN} = V_{SS}$ or V_{CC} device in Stand-by mode		± 2	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ or V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	V_{CC}=5V, f_c=400kHz (rise/fall time < 30ns)		2	mA
I_{CC1}	Stand-by Supply Current	$V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 5$ V		10	µA
V_{IL}	Input Low Voltage (E2, E1, E0, SCL, SDA)		–0.3	$0.3V_{CC}$	V
	Input Low Voltage ($\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E2, E1, E0, SCL, SDA, $\overline{WC}$)		$0.7V_{CC}$	V_{CC}+1	V
V_{OL}	Output Low Voltage	$I_{OL} = 3$ mA, $V_{CC} = 5$ V		0.4	V

Table 13. DC Characteristics (M24Cxx-W)

Symbol	Parameter	Test Condition (in addition to those in Table 8)	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA, E2, E1, E0)	$V_{IN} = V_{SS}$ or V_{CC} device in Stand-by mode		± 2	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ or V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	V_{CC} =2.5V, f_c=400kHz (rise/fall time < 30ns)		1	mA
I_{CC1}	Stand-by Supply Current	$V_{IN} = V_{SS}$ or V_{CC} , $V_{CC} = 2.5$ V		2	µA
V_{IL}	Input Low Voltage (E2, E1, E0, SCL, SDA)		–0.3	$0.3V_{CC}$	V
	Input Low Voltage ($\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E2, E1, E0, SCL, SDA, $\overline{WC}$)		$0.7V_{CC}$	V_{CC}+1	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA, $V_{CC} = 2.5$ V		0.4	V

Table 14. DC Characteristics (M24Cxx-R)

Symbol	Parameter	Test Condition (in addition to those in Table 9)	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA, E2, E1, E0)	$V_{IN} = V_{SS}$ or V_{CC} device in Stand-by mode		± 2	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ or V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	V_{CC}=1.8V, f_C=100kHz (rise/fall time < 30ns)		0.8	mA
I_{CC1}	Stand-by Supply Current	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8 V		0.2	µA
V_{IL}	Input Low Voltage (E2, E1, E0, SCL, SDA)		– 0.3	0.3 V_{CC}	V
	Input Low Voltage ($\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E2, E1, E0, SCL, SDA, $\overline{WC}$)		0.7V_{CC}	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 0.7 mA, V_{CC} = 1.8 V		0.2	V

Table 15. AC Characteristics (M24Cxx, M24Cxx-W)

Test conditions specified in Table 10 and Table 7 or 8					
Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock Frequency		400	kHz
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1300		ns
t_{DL1DL2} [2]	t_F	SDA Fall Time	20	300	ns
t_{DXCX}	$t_{SU:DAT}$	Data In Set Up Time	100		ns
t_{CLDX}	$t_{HD:DAT}$	Data In Hold Time	0		ns
t_{CLQX}	t_{DH}	Data Out Hold Time	200		ns
t_{CLQV} [3]	t_{AA}	Clock Low to Next Data Valid (Access Time)	200	900	ns
t_{CHDX} [1]	$t_{SU:STA}$	Start Condition Set Up Time	600		ns
t_{DLCL}	$t_{HD:STA}$	Start Condition Hold Time	600		ns
t_{CHDH}	$t_{SU:STO}$	Stop Condition Set Up Time	600		ns
t_{DHDL}	t_{BUF}	Time between Stop Condition and Next Start Condition	1300		ns
t_W	t_{WR}	Write Time		5 or[4] 10	ms

Note: 1. For a reSTART condition, or following a Write cycle.
2. Sampled only, not 100% tested.
3. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
4. The Write Time of 5 ms only applies to devices bearing the process letter "B" in the package marking (on the top side of the package), otherwise (for devices bearing the process letter "N") the Write Time is 10 ms. For further details, please contact your nearest ST sales office, and ask for a copy of the Product Change Notice PCEE0036.

Table 16. AC Characteristics (M24Cxx-R)

Test conditions specified in Table 10 and Table 9					
Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock Frequency		400	kHz
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1300		ns
t_{DL1DL2} [2]	t_F	SDA Fall Time	20	300	ns
t_{DXCX}	$t_{SU:DAT}$	Data In Set Up Time	100		ns
t_{CLDX}	$t_{HD:DAT}$	Data In Hold Time	0		ns
t_{CLQX}	t_{DH}	Data Out Hold Time	200		ns
t_{CLQV} [3]	t_{AA}	Clock Low to Next Data Valid (Access Time)	200	900	ns
t_{CHDX} [1]	$t_{SU:STA}$	Start Condition Set Up Time	600		ns
t_{DLCL}	$t_{HD:STA}$	Start Condition Hold Time	600		ns
t_{CHDH}	$t_{SU:STO}$	Stop Condition Set Up Time	600		ns
t_{DHDL}	t_{BUF}	Time between Stop Condition and Next Start Condition	1300		ns
t_W	t_{WR}	Write Time		10	ms

Note: 1. For a reSTART condition, or following a Write cycle.
2. Sampled only, not 100% tested.
3. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.

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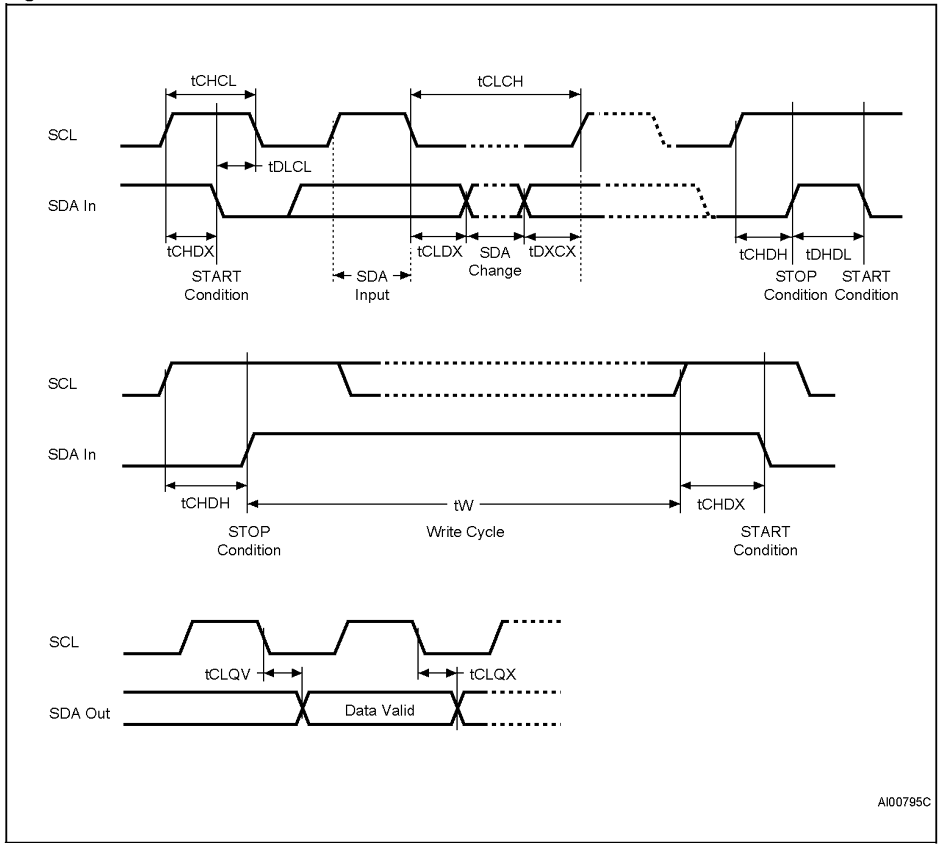
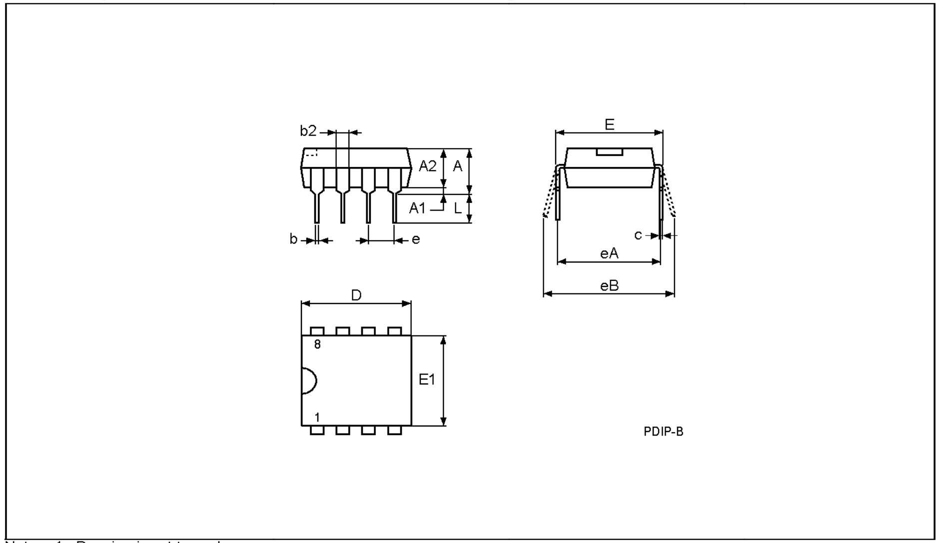
Figure 11. AC Waveforms



PACKAGE MECHANICAL

PDIP8 – 8 pin Plastic DIP, 0.25mm lead frame, Package Outline



Notes: 1. Drawing is not to scale.

PDIP8 – 8 pin Plastic DIP, 0.25mm lead frame, Package Mechanical Data

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			5.33			0.210
A1		0.38			0.015	
A2	3.30	2.92	4.95	0.130	0.115	0.195
b	0.46	0.36	0.56	0.018	0.014	0.022
b2	1.52	1.14	1.78	0.060	0.045	0.070
c	0.25	0.20	0.36	0.010	0.008	0.014
D	9.27	9.02	10.16	0.365	0.355	0.400
E	7.87	7.62	8.26	0.310	0.300	0.325
E1	6.35	6.10	7.11	0.250	0.240	0.280
e	2.54	–	–	0.100	–	–
eA	7.62	–	–	0.300	–	–
eB			10.92			0.430
L	3.30	2.92	3.81	0.130	0.115	0.150

LT1308A/LT1308B

High Current, Micropower Single Cell, 600kHz DC/DC Converters

FEATURES

- **5V at 1A from a Single Li-Ion Cell**
- **5V at 800mA in SEPIC Mode from Four NiCd Cells**
- **Fixed Frequency Operation: 600kHz**
- **Boost Converter Outputs up to 34V**
- **Thin 1.1mm Height TSSOP Packaging Available**
- Starts into Heavy Loads
- Automatic Burst Mode™ Operation at Light Load (LT1308A)
- Continuous Switching at Light Loads (LT1308B)
- Low V_{CESAT} Switch: 300mV at 2A
- Pin-for-Pin Upgrade Compatible with LT1308
- Lower Quiescent Current in Shutdown: 1µA (Max)
- Improved Accuracy Low-Battery Detector Reference: 200mV ±2%

APPLICATIONS

- GSM/CDMA Phones
- Digital Cameras
- LCD Bias Supplies
- Answer-Back Pagers
- GPS Receivers
- Battery Backup Supplies
- Handheld Computers

DESCRIPTION

The LT®1308A/LT1308B are micropower, fixed frequency step-up DC/DC converters that operate over a 1V to 10V input voltage range. They are improved versions of the LT1308 and are recommended for use in new designs. The LT1308A features automatic shifting to power saving Burst Mode operation at light loads and consumes just 140µA at no load. The LT1308B features continuous switching at light loads and operates at a quiescent current of 2.5mA. Both devices consume less than 1µA in shutdown.

Low-battery detector accuracy is significantly tighter than the LT1308. The 200mV reference is specified at ±2% at room and ±3% over temperature. The shutdown pin enables the device when it is tied to a 1V or higher source and does not need to be tied to V_{IN} as on the LT1308. An internal V_C clamp results in improved transient response and the switch voltage rating has been increased to 36V, enabling higher output voltage applications.

The LT1308A/LT1308B are available in the 8-lead SO and the 14-lead TSSOP packages.

TYPICAL APPLICATION

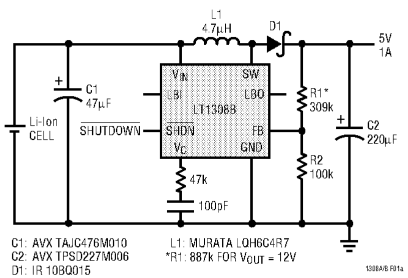
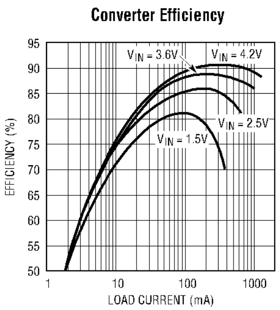


Figure 1. LT1308B Single Li-Ion Cell to 5V/1A DC/DC Converter

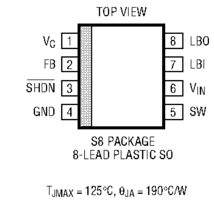


ABSOLUTE MAXIMUM RATINGS (Note 1)

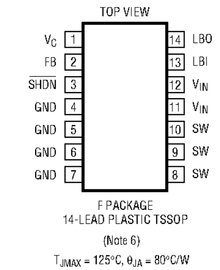
V_{IN}, $\overline{SHDN}$, LBO Voltage 10V
SW Voltage .... –0.4V to 36V
FB Voltage .... V_{IN} + 1V
V_C Voltage 2V
LBI Voltage .... –0.1V to 1V
Current into FB Pin .... ±1mA

Operating Temperature Range
Commercial .... 0°C to 70°C
Extended Commerial (Note 2) .... –40°C to 85°C
Industrial .... –40°C to 85°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER	
LT1308ACS8	
LT1308AIS8	
LT1308BCS8	
LT1308BIS8	
S8 PART MARKING	
1308A	1308B
1308AI	1308BI



ORDER PART NUMBER
LT1308ACF
LT1308BCF

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. Commercial Grade 0°C to 70°C. V_{IN} = 1.1V, $V_{\overline{SHDN}}$ = V_{IN}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	Not Switching, LT1308A Switching, LT1308B $V_{\overline{SHDN}}$ = 0V (LT1308A/LT1308B)			140 2.5 0.01	240 4 1	µA mA µA
V_{FB}	Feedback Voltage		●	1.20	1.22	1.24	V
I_B	FB Pin Bias Current	(Note 3)	●		27	80	nA
	Reference Line Regulation	1.1V ≤ V_{IN} ≤ 2V 2V ≤ V_{IN} ≤ 10V	●		0.03 0.01	0.4 0.2	%/V %/V
	Minimum Input Voltage				0.92	1	V
g_m	Error Amp Transconductance	ΔI = 5µA			60		µmhos
A_V	Error Amp Voltage Gain				100		V/V
f_{OSC}	Switching Frequency	V_{IN} = 1.2V	●	500	600	700	kHz
	Maximum Duty Cycle		●	82	90		%
	Switch Current Limit	Duty Cyle = 30% (Note 4)		2	3	4.5	A
	Switch V_{CESAT}	I_{SW} = 2A (25°C, 0°C), V_{IN} = 1.5V I_{SW} = 2A (70°C), V_{IN} = 1.5V			290 330	350 400	mV mV
	Burst Mode Operation Switch Current Limit (LT1308A)	V_{IN} = 2.5V, Circuit of Figure 1			400		mA