ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. Commercial Grade 0°C to 70°C. V_{IN} = 1.1V, $V_{\overline{SHDN}}$ = V_{IN}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Shutdown Pin Current	$V_{\overline{SHDN}}$ = 1.1V	●		2	5	µA
		$V_{\overline{SHDN}}$ = 6V	●		20	35	µA
		$V_{\overline{SHDN}}$ = 0V	●		0.01	0.1	µA
	LBI Threshold Voltage			196	200	204	mV
			●	194	200	206	mV
	LBO Output Low	I_{SINK} = 50µA	●		0.1	0.25	V
	LBO Leakage Current	V_{LBI} = 250mV, V_{LBO} = 5V	●		0.01	0.1	µA
	LBI Input Bias Current (Note 5)	V_{LBI} = 150mV			33	100	nA
	Low-Battery Detector Gain				3000		V/V
	Switch Leakage Current	V_{SW} = 5V	●		0.01	10	µA

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. Industrial Grade –40°C to 85°C. V_{IN} = 1.2V, $V_{\overline{SHDN}}$ = V_{IN}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	Not Switching, LT1308A	●		140	240	µA
		Switching, LT1308B	●		2.5	4	mA
		$V_{\overline{SHDN}}$ = 0V (LT1308A/LT1308B)	●		0.01	1	µA
V_{FB}	Feedback Voltage		●	1.19	1.22	1.25	V
I_B	FB Pin Bias Current	(Note 3)	●		27	80	nA
	Reference Line Regulation	1.1V ≤ V_{IN} ≤ 2V	●		0.05	0.4	%/V
		2V ≤ V_{IN} ≤ 10V	●		0.01	0.2	%/V
	Minimum Input Voltage				0.92	1	V
g_m	Error Amp Transconductance	ΔI = 5µA			60		µmhos
A_V	Error Amp Voltage Gain				100		V/V
f_{OSC}	Switching Frequency		●	500	600	750	kHz
	Maximum Duty Cycle		●	82	90		%
	Switch Current Limit	Duty Cyle = 30% (Note 4)		2	3	4.5	A
	Switch V_{CESAT}	I_{SW} = 2A (25°C, –40°C), V_{IN} = 1.5V			290	350	mV
		I_{SW} = 2A (85°C), V_{IN} = 1.5V			330	400	mV
	Burst Mode Operation Switch Current Limit (LT1308A)	V_{IN} = 2.5V, Circuit of Figure 1			400		mA
	Shutdown Pin Current	$V_{\overline{SHDN}}$ = 1.1V	●		2	5	µA
		$V_{\overline{SHDN}}$ = 6V	●		20	35	µA
		$V_{\overline{SHDN}}$ = 0V			0.01	0.1	µA
	LBI Threshold Voltage			196	200	204	mV
			●	193	200	207	mV
	LBO Output Low	I_{SINK} = 50µA	●		0.1	0.25	V
	LBO Leakage Current	V_{LBI} = 250mV, V_{LBO} = 5V	●		0.01	0.1	µA
	LBI Input Bias Current (Note 5)	V_{LBI} = 150mV			33	100	nA
	Low-Battery Detector Gain				3000		V/V
	Switch Leakage Current	V_{SW} = 5V	●		0.01	10	µA

ELECTRICAL CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LT1308ACS8, LT1308ACF, LT1308BCS8 and LT1308BCF are designed, characterized and expected to meet the industrial temperature limits, but are not tested at –40°C and 85°C. I grade devices are guaranteed over the –40°C to 85°C operating temperature range.

Note 3: Bias current flows into FB pin.

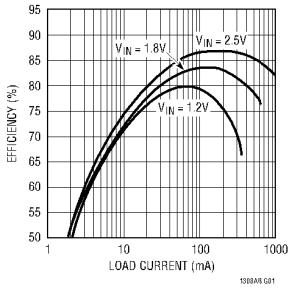
Note 4: Switch current limit guaranteed by design and/or correlation to static tests. Duty cycle affects current limit due to ramp generator (see Block Diagram).

Note 5: Bias current flows out of LBI pin.

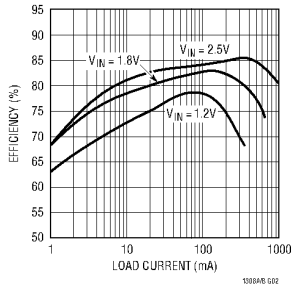
Note 6: Connect the four GND pins (Pins 4–7) together at the device. Similarly, connect the three SW pins (Pins 8–10) together and the two V_{IN} pins (Pins 11, 12) together at the device.

TYPICAL PERFORMANCE CHARACTERISTICS

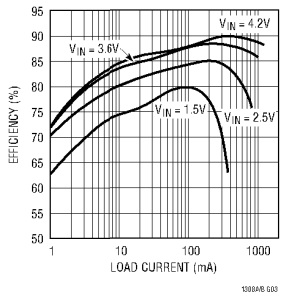
LT1308B
3.3V Output Efficiency



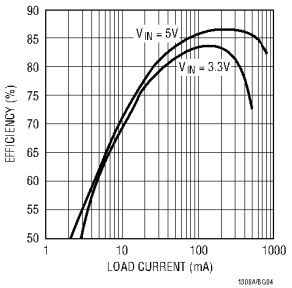
LT1308A
3.3V Output Efficiency



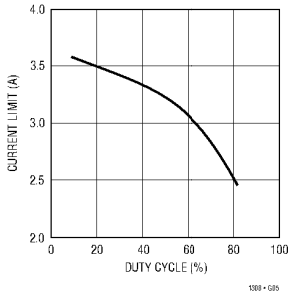
LT1308A
5V Output Efficiency



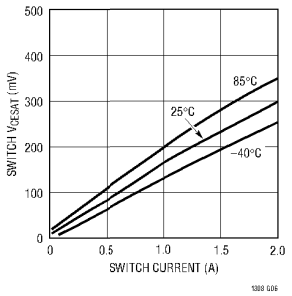
LT1308B
12V Output Efficiency



Switch Current Limit vs
Duty Cycle

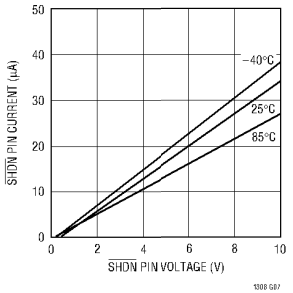


Switch Saturation Voltage
vs Current

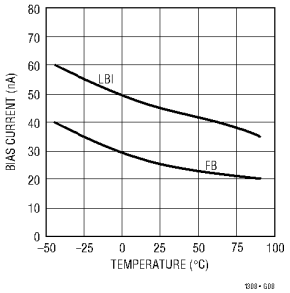


TYPICAL PERFORMANCE CHARACTERISTICS

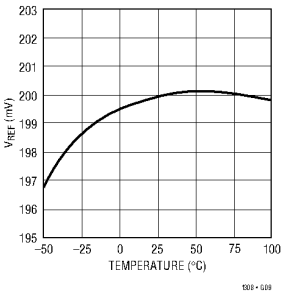
$\overline{SHDN}$ Pin Bias Current vs Voltage



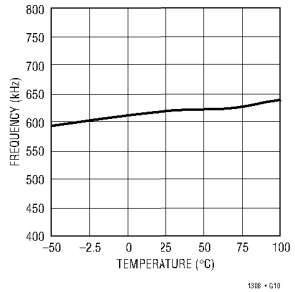
FB, LBI Bias Current vs Temperature



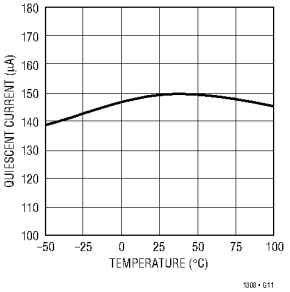
Low Battery Detector Reference vs Temperature



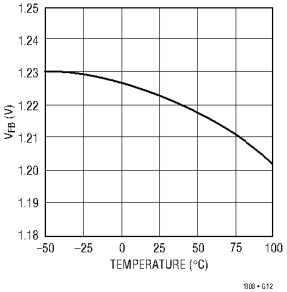
Oscillator Frequency vs Temperature



LT1308A Quiescent Current vs Temperature



Feedback Pin Voltage vs Temperature



Tournez la page S.V.P.

PIN FUNCTIONS

SO-8 Package

V_C (Pin 1): Compensation Pin for Error Amplifier. Connect a series RC from this pin to ground. Typical values are 47kΩ and 100pF. Minimize trace area at V_C.

FB (Pin 2): Feedback Pin. Reference voltage is 1.22V. Connect resistive divider tap here. Minimize trace area at FB. Set V_{OUT} according to: $V_{OUT} = 1.22V(1 + R1/R2)$.

$\overline{SHDN}$ (Pin 3): Shutdown. Ground this pin to turn off switcher. To enable, tie to 1V or more. $\overline{SHDN}$ does not need to be at V_{IN} to enable the device.

GND (Pin 4): Ground. Connect directly to local ground plane. Ground plane should enclose all components associated with the LT1308. PCB copper connected to Pin 4 also functions as a heat sink. Maximize this area to keep chip heating to a minimum.

SW (Pin 5): Switch Pin. Connect inductor/diode here. Minimize trace area at this pin to keep EMI down.

V_{IN} (Pin 6): Supply Pin. Must have local bypass capacitor right at the pin, connected directly to ground.

LBI (Pin 7): Low-Battery Detector Input. 200mV reference. Voltage on LBI must stay between –100mV and 1V. Low-battery detector does not function with $\overline{SHDN}$ pin grounded. Float LBI pin if not used.

LBO (Pin 8): Low-Battery Detector Output. Open collector, can sink 50µA. A 220kΩ pull-up is recommended. LBO is high impedance when $\overline{SHDN}$ is grounded.

TSSOP Package

V_C (Pin 1): Compensation Pin for Error Amplifier. Connect a series RC from this pin to ground. Typical values are 47kΩ and 100pF. Minimize trace area at V_C.

FB (Pin 2): Feedback Pin. Reference voltage is 1.22V. Connect resistive divider tap here. Minimize trace area at FB. Set V_{OUT} according to: $V_{OUT} = 1.22V(1 + R1/R2)$.

$\overline{SHDN}$ (Pin 3): Shutdown. Ground this pin to turn off switcher. To enable, tie to 1V or more. $\overline{SHDN}$ does not need to be at V_{IN} to enable the device.

GND (Pins 4, 5, 6, 7): Ground. Connect directly to local ground plane. Ground plane should enclose all components associated with the LT1308. PCB copper connected to these pins also functions as a heat sink. Connect all pins to ground copper to get the best heat transfer. This keeps chip heating to a minimum.

SW (Pins 8, 9, 10): Switch Pins. Connect inductor/diode here. Minimize trace area at these pins to keep EMI down. Connect all SW pins together at the package.

V_{IN} (Pins 11, 12): Supply Pins. Must have local bypass capacitor right at the pins, connected directly to ground. Connect both V_{IN} pins together at the package.

LBI (Pin 13): Low-Battery Detector Input. 200mV reference. Voltage on LBI must stay between –100mV and 1V. Low-battery detector does not function with $\overline{SHDN}$ pin grounded. Float LBI pin if not used.

LBO (Pin 14): Low-Battery Detector Output. Open collector, can sink 50µA. A 220kΩ pull-up is recommended. LBO is high impedance when $\overline{SHDN}$ is grounded.

BLOCK DIAGRAMS

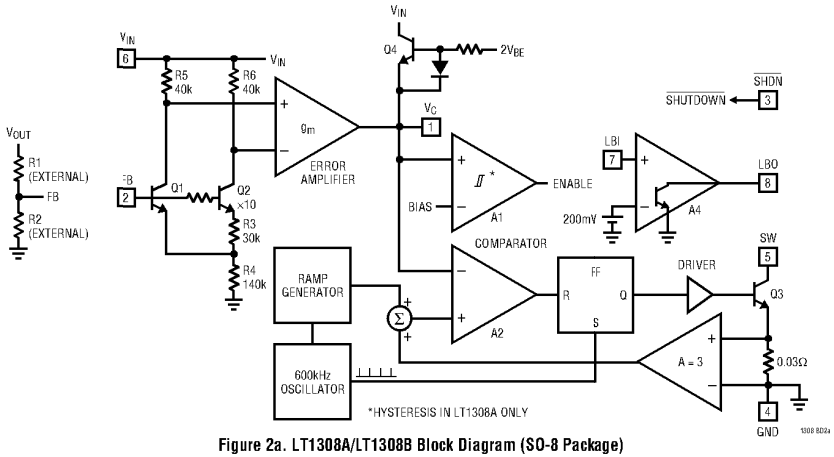


Figure 2a. LT1308A/LT1308B Block Diagram (SO-8 Package)

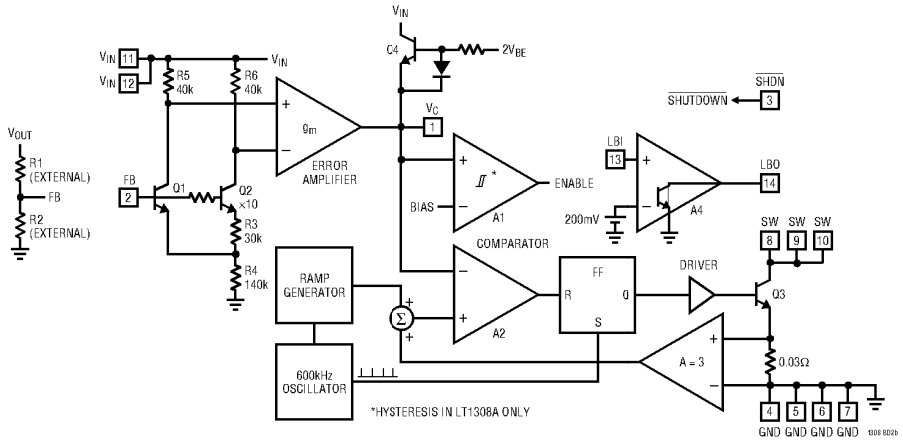


Figure 2b. LT1308A/LT1308B Block Diagram (TSSOP Package)

APPLICATIONS INFORMATION

OPERATION

The LT1308A combines a current mode, fixed frequency PWM architecture with Burst Mode micropower operation to maintain high efficiency at light loads. Operation can be best understood by referring to the block diagram in Figure 2. Q1 and Q2 form a bandgap reference core whose loop is closed around the output of the converter. When V_{IN} is 1V, the feedback voltage of 1.22V, along with an 80mV drop across R5 and R6, forward biases Q1 and Q2's base collector junctions to 300mV. Because this is not enough to saturate either transistor, FB can be at a higher voltage than V_{IN}. When there is no load, FB rises slightly above 1.22V, causing V_C (the error amplifier's output) to decrease. When V_C reaches the bias voltage on hysteretic comparator A1, A1's output goes low, turning off all circuitry except the input stage, error amplifier and low-battery detector. Total current consumption in this state is 140µA. As output loading causes the FB voltage to decrease, A1's output goes high, enabling the rest of the IC. Switch current is limited to approximately 400mA initially after A1's output goes high. If the load is light, the output voltage (and FB voltage) will increase until A1's output goes low, turning off the rest of the LT1308A. Low frequency ripple voltage appears at the output. The ripple frequency is dependent on load current and output capacitance. This Burst Mode operation keeps the output regulated and reduces average current into the IC, resulting in high efficiency even at load currents of 1mA or less.

If the output load increases sufficiently, A1's output remains high, resulting in continuous operation. When the LT1308A is running continuously, peak switch current is controlled by V_C to regulate the output voltage. The switch is turned on at the beginning of each switch cycle. When the summation of a signal representing switch current and a ramp generator (introduced to avoid subharmonic oscillations at duty factors greater than 50%) exceeds the V_C signal, comparator A2 changes state, resetting the flip-flop and turning off the switch. Output voltage increases as switch current is increased. The output, attenuated by a resistor divider, appears at the FB pin, closing the overall loop. Frequency compensation is provided by an external series RC network connected between the V_C pin and ground.

Low-battery detector A4's open-collector output (LBO) pulls low when the LBI pin voltage drops below 200mV. There is no hysteresis in A4, allowing it to be used as an amplifier in some applications. The entire device is disabled when the $\overline{SHDN}$ pin is brought low. To enable the converter, $\overline{SHDN}$ must be at 1V or greater. It need not be tied to V_{IN} as on the LT1308.

The LT1308B differs from the LT1308A in that there is no hysteresis in comparator A1. Also, the bias point on A1 is set lower than on the LT1308B so that switching can occur at inductor current less than 100mA. Because A1 has no hysteresis, there is no Burst Mode operation at light loads and the device continues switching at constant frequency. This results in the absence of low frequency output voltage ripple at the expense of efficiency.

The difference between the two devices is clearly illustrated in Figure 3. The top two traces in Figure 3 shows an LT1308A/LT1308B circuit, using the components indicated in Figure 1, set to a 5V output. Input voltage is 3V. Load current is stepped from 50mA to 800mA for both circuits. Low frequency Burst Mode operation voltage ripple is observed on Trace A, while none is observed on Trace B.

At light loads, the LT1308B will begin to skip alternate cycles. The load point at which this occurs can be decreased by increasing the inductor value. However, output ripple will continue to be significantly less than the LT1308A output ripple. Further, the LT1308B can be forced into micropower mode, where I_Q falls from 3mA to 200µA by sinking 40µA or more out of the V_C pin. This stops switching by causing A1's output to go low.

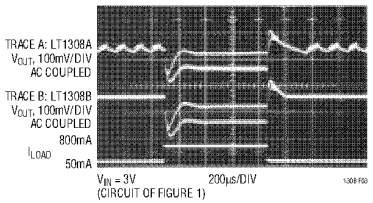


Figure 3. LT1308A Exhibits Burst Mode Operation Output Voltage Ripple at 50mA Load, LT1308B Does Not

APPLICATIONS INFORMATION

Waveforms for a LT1308B 5V to 12V boost converter using a 10µF ceramic output capacitor are pictured in Figures 4 and 5. In Figure 4, the converter is operating in continuous mode, delivering a load current of approximately 500mA. The top trace is the output. The voltage increases as inductor current is dumped into the output capacitor during the switch off time, and the voltage decreases when the switch is on. Ripple voltage is in this case due to capacitance, as the ceramic capacitor has little ESR. The middle trace is the switch voltage. This voltage alternates between a V_{CESAT} and V_{OUT} plus the diode drop. The lower trace is the switch current. At the beginning of the switch cycle, the current is 1.2A. At the end of the switch on time, the current has increased to 2A, at which point the switch turns off and the inductor current flows into the output capacitor through the diode. Figure 5 depicts converter waveforms at a light load. Here the converter operates in discontinuous mode. The inductor current reaches zero during the switch off time, resulting in some ringing at the switch node. The ring frequency is set by switch capacitance, diode capacitance and inductance. This ringing has little energy, and its sinusoidal shape suggests it is free from harmonics. Minimizing the copper area at the switch node will prevent this from causing interference problems.

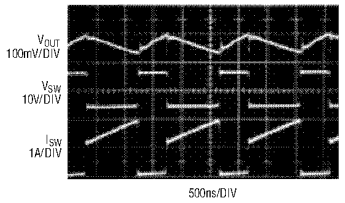


Figure 4. 5V to 12V Boost Converter Waveforms in Continuous Mode. 10µF Ceramic Capacitor Used at Output

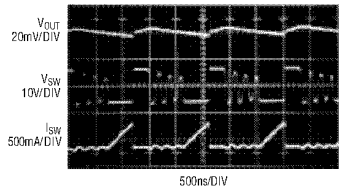


Figure 5. Converter Waveforms in Discontinuous Mode

LAYOUT HINTS

The LT1308A/LT1308B switch current at high speed, mandating careful attention to layout for proper performance. *You will not get advertised performance with careless layout.* Figure 6 shows recommended component placement for an SO-8 package boost (step-up) converter. Follow this closely in your PC layout. Note the direct path of the switching loops. Input capacitor C1 *must* be placed close (<5mm) to the IC package. As little as 10mm of wire or PC trace from C_{IN} to V_{IN} will cause problems such as inability to regulate or oscillation.

The negative terminal of output capacitor C2 should tie close to the ground pin(s) of the LT1308A/LT1308B. Doing this reduces dI/dt in the ground copper which keeps high frequency spikes to a minimum. The DC/DC converter ground should tie to the PC board ground plane at one place only, to avoid introducing dI/dt in the ground plane.

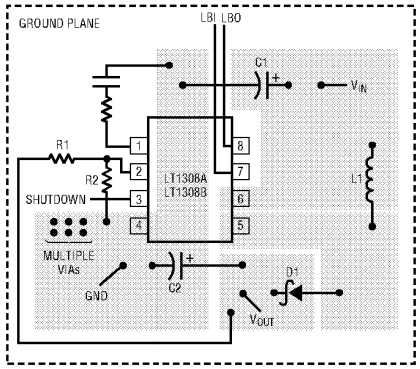


Figure 6. Recommended Component Placement for SO-8 Package Boost Converter. Note Direct High Current Paths Using Wide PC Traces. Minimize Trace Area at Pin 1 (V_C) and Pin 2 (FB). Use Multiple Vias to Tie Pin 4 Copper to Ground Plane. Use Vias at One Location Only to Avoid Introducing Switching Currents into the Ground Plane

Figure 7 shows recommended component placement for a boost converter using the TSSOP package. Placement is similar to the SO-8 package layout.

Tournez la page S.V.P.

APPLICATIONS INFORMATION

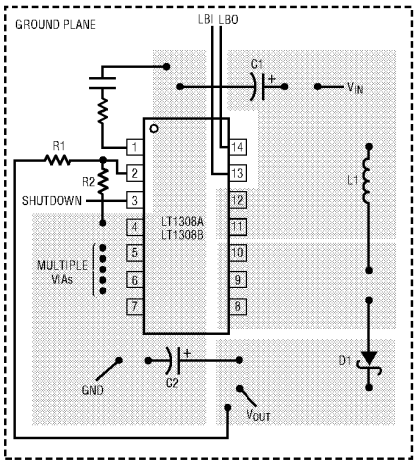


Figure 7. Recommended Component Placement for TSSOP Boost Converter. Placement is Similar to Figure 4.

A SEPIC (Single-Ended Primary Inductance Converter) schematic is shown in Figure 8. This converter topology produces a regulated output over an input voltage range that spans (i.e., can be higher or lower than) the output. Recommended component placement for an SO-8 package SEPIC is shown in Figure 9.

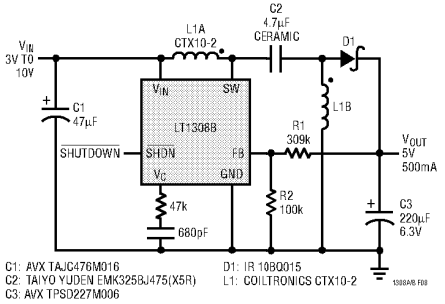


Figure 8. SEPIC (Single-Ended Primary Inductance Converter) Converts 3V to 10V Input to a 5V/500mA Regulated Output

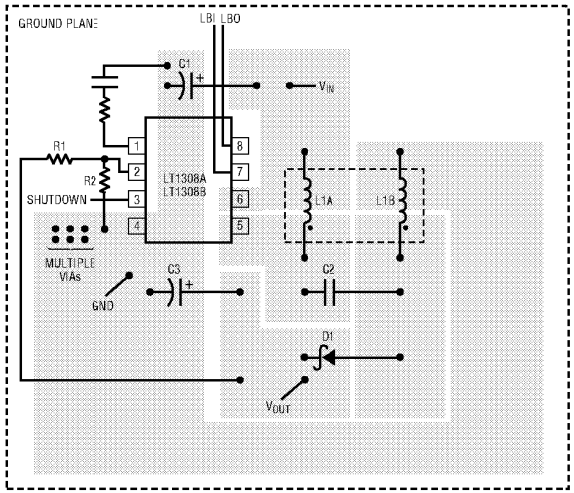


Figure 9. Recommended Component Placement for SEPIC

APPLICATIONS INFORMATION

$\overline{SHDN}$ PIN

The LT1308A/LT1308B $\overline{SHDN}$ pin is improved over the LT1308. The pin does not require tying to V_{IN} to enable the device, but needs only a logic level signal. The voltage on the $\overline{SHDN}$ pin can vary from 1V to 10V independent of V_{IN}. Further, floating this pin has the same effect as grounding, which is to shut the device down, reducing current drain to 1µA or less.

LOW-BATTERY DETECTOR

The low-battery detector on the LT1308A/LT1308B features improved accuracy and drive capability compared to the LT1308. The 200mV reference has an accuracy of ±2% and the open-collector output can sink 50µA. The LT1308A/LT1308B low-battery detector is a simple PNP input gain stage with an open-collector NPN output. The negative input of the gain stage is tied internally to a 200mV reference. The positive input is the LBI pin. Arrangement as a low-battery detector is straightforward. Figure 10 details hookup. R1 and R2 need only be low enough in value so that the bias current of the LBI pin doesn't cause large errors. For R2, 100k is adequate. The 200mV reference can also be accessed as shown in Figure 11.

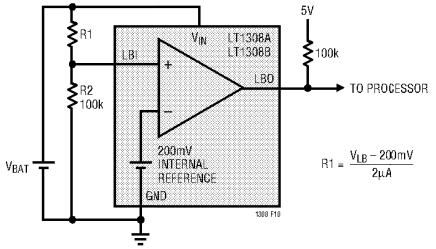


Figure 10. Setting Low-Battery Detector Trip Point

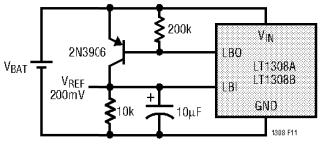


Figure 11. Accessing 200mV Reference

A cross plot of the low-battery detector is shown in Figure 12. The LBI pin is swept with an input which varies from 195mV to 205mV, and LBO (with a 100k pull-up resistor) is displayed.

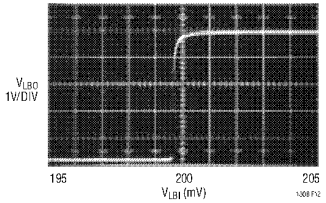


Figure 12. Low-Battery Detector Input/Output Characteristic

START-UP

The LT1308A/LT1308B can start up into heavy loads, unlike many CMOS DC/DC converters that derive operating voltage from the output (a technique known as "bootstrapping"). Figure 13 details start-up waveforms of Figure 1's circuit with a 20Ω load and V_{IN} of 1.5V. Inductor current rises to 3.5A as the output capacitor is charged. After the output reaches 5V, inductor current is about 1A. In Figure 14, the load is 5Ω and input voltage is 3V. Output voltage reaches 5V in 500µs after the device is enabled. Figure 15 shows start-up behavior of Figure 5's SEPIC circuit, driven from a 9V input with a 10Ω load. The output reaches 5V in about 1ms after the device is enabled.

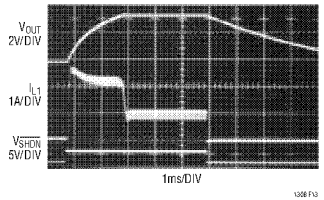


Figure 13. 5V Boost Converter of Figure 1. Start-Up from 1.5V Input into 20Ω Load

APPLICATIONS INFORMATION

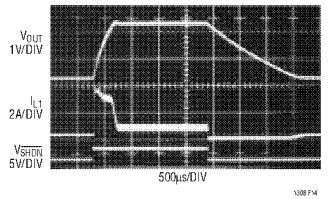


Figure 14. 5V Boost Converter of Figure 1. Start-Up from 3V Input into 5Ω Load

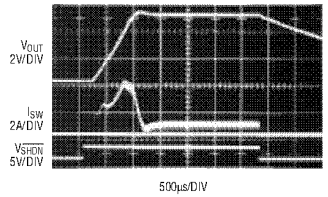


Figure 15. 5V SEPIC Start-Up from 9V Input into 10Ω Load

Soft-Start

In some cases it may be undesirable for the LT1308A/LT1308B to operate at current limit during start-up, e.g., when operating from a battery composed of alkaline cells. The inrush current may cause sufficiency internal voltage drop to trigger a low-battery indicator. A programmable soft-start can be implemented with 4 discrete components. A 5V to 12V boost converter using the LT1308B is detailed in Figure 16. C4 differentiates V_{OUT}, causing a current to flow into R3 as V_{OUT} increases. When this current exceeds 0.7V/33k, or 21µA, current flows into the base of Q1. Q1's collector then pulls current out the V_C pin, creating a feedback loop where the slope of V_{OUT} is limited as follows:

$$\frac{\Delta V_{OUT}}{\Delta t} = \frac{0.7V}{33k \bullet C4}$$

With C4 = 33nF, V_{OUT}/t is limited to 640mV/ms. Start-up waveforms for Figure 16's circuit are pictured in Figure 17. Without the soft-start circuit implemented, the inrush current reaches 3A. The circuit reaches final output voltage in approximately 250µs. Adding the soft-start components reduces inductor current to less than 1A, as detailed in Figure 18, while the time required to reach final output voltage increases to about 15ms. C4 can be adjusted to achieve any output slew rate desired.

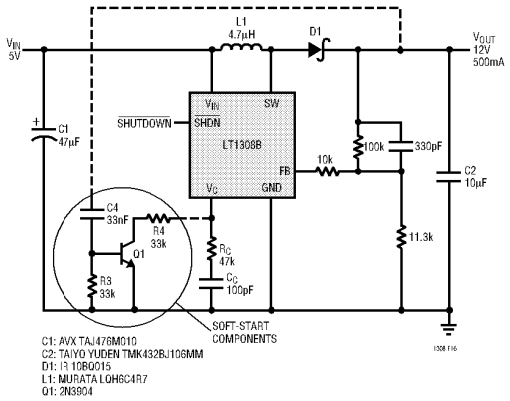


Figure 16. 5V to 12V Boost Converter with Soft-Start Components Q1, C4, R3 and R4.

APPLICATIONS INFORMATION

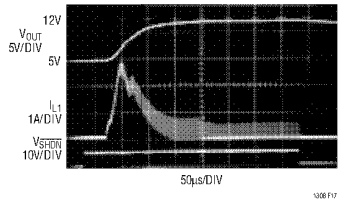


Figure 17. Start-Up Waveforms of Figure 16's Circuit without Soft-Start Components

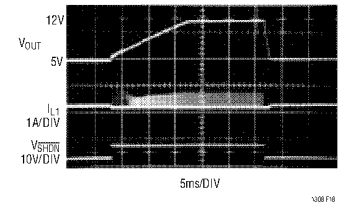


Figure 18. Start-Up Waveforms of Figure 16's Circuit with Soft-Start Components Added

COMPONENT SELECTION

Diodes

We have found ON Semiconductor MBRS130 and International Rectifier 10BQ015 to perform well. For applications where V_{OUT} exceeds 30V, use 40V diodes such as MBRS140 or 10BQ040.

Height limited applications may benefit from the use of the MBRM120. This component is only 1mm tall and offers performance similar to the MBRS130.

Inductors

Suitable inductors for use with the LT1308A/LT1308B must fulfill two requirements. First, the inductor must be able to handle current of 2A steady-state, as well as support transient and start-up current over 3A without inductance decreasing by more than 50% to 60%. Second, the DCR of the inductor should have low DCR, under 0.05Ω so that copper loss is minimized. Acceptable inductance values range between 2µH and 20µH, with 4.7µH best for most applications. Lower value inductors are physically smaller than higher value inductors for the same current capability.

Table 1 lists some inductors we have found to perform well in LT1308A/LT1308B application circuits. This is not an exclusive list.

Table 1

VENDOR	PART NO.	VALUE	PHONE NO.
Murata	LQH6C4R7	4.7µH	770-436-1300
Sumida	CDRH734R7	4.7µH	847-956-0666
Coiltronics	CTX5-1	5µH	561-241-7876
Coilcraft	LPO2506IB-472	4.7µH	847-639-6400

Capacitors

Equivalent Series Resistance (ESR) is the main issue regarding selection of capacitors, especially the output capacitors.

The output capacitors specified for use with the LT1308A/LT1308B circuits have low ESR and are specifically designed for power supply applications. Output voltage ripple of a boost converter is equal to ESR multiplied by switch current. The performance of the AVX TPSD227M006 220µF tantalum can be evaluated by referring to Figure 3. When the load is 800mA, the peak switch current is approximately 2A. Output voltage ripple is about 60mV_{P-P}, so the ESR of the output capacitor is 60mV/2A or 0.03Ω. Ripple can be further reduced by paralleling ceramic units.

Table 2 lists some capacitors we have found to perform well in the LT1308A/LT1308B application circuits. This is not an exclusive list.

Table 2

VENDOR	SERIES	PART NO.	VALUE	PHONE NO.
AVX	TPS	TPSD227M006	220µF, 6V	803-448-9411
AVX	TPS	TPSD107M010	100µF, 10V	803-448-9411
Taiyo Yuden	X5R	LMK432BJ226	22µF, 10V	408-573-4150
Taiyo Yuden	X5R	TMK432BJ106	10µF, 25V	408-573-4150

Tournez la page S.V.P.

APPLICATIONS INFORMATION

Ceramic Capacitors

Multilayer ceramic capacitors have become popular, due to their small size, low cost, and near-zero ESR. Ceramic capacitors can be used successfully in LT1308A/LT1308B designs provided loop stability is considered. A tantalum capacitor has some ESR and this causes an "ESR zero" in the regulator loop. This zero is beneficial to loop stability. Ceramics do not have appreciable ESR, so the zero is lost when they are used. However, the LT1308A/LT1308B have external compensation pin (V_C) so component values can be adjusted to achieve stability. A phase lead capacitor can also be used to tune up load step response to optimum levels, as detailed in the following paragraphs.

Figure 19 details a 5V to 12V boost converter using either a tantalum or ceramic capacitor for C2. The input capacitor has little effect on loop stability, as long as minimum capacitance requirements are met. The phase lead capacitor C_{PL} parallels feedback resistor R1. Figure 20 shows load step response of a 50mA to 500mA load step using a 47µF tantalum capacitor at the output. Without the phase lead capacitor, there is some ringing, suggesting the phase margin is low. C_{PL} is then added, and response to the same load step is pictured in Figure 21. Some phase margin is restored, improving the response. Next, C2 is replaced by a 10µF, X5R dielectric, ceramic capacitor.

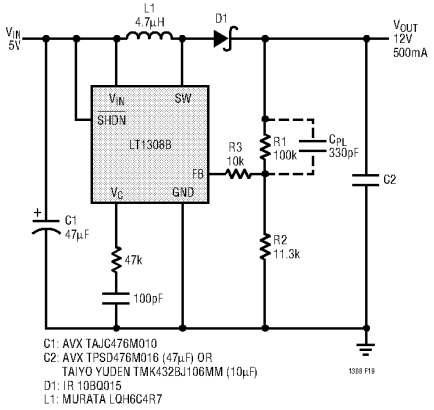


Figure 19. 5V to 12V Boost Converter

Without C_{PL}, load step response is pictured in Figure 22. Although the output settles faster than the tantalum case, there is appreciable ringing, again suggesting phase margin is low. Figure 23 depicts load step response using the 10µF ceramic output capacitor and C_{PL}. Response is clean and no ringing is evident. Ceramic capacitors have the added benefit of lowering ripple at the switching frequency due to their very low ESR. By applying C_{PL} in tandem with the series RC at the V_C pin, loop response can be tailored to optimize response using ceramic output capacitors.

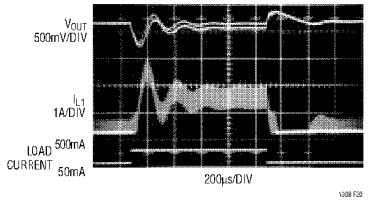


Figure 20. Load Step Response of LT1308B 5V to 12V Boost Converter with 47µF Tantalum Output Capacitor

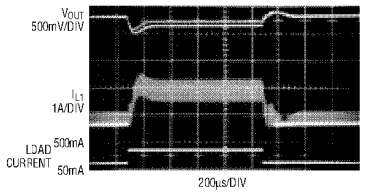


Figure 21. Load Step Response with 47µF Tantalum Output Capacitor and Phase Lead Capacitor C_{PL}

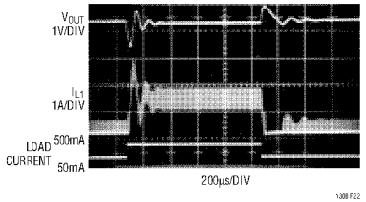


Figure 22. Load Step Response with 10µF X5R Ceramic Output Capacitor

SEPIC Constant-Current/ Constant-Voltage Battery Charger

FEATURES

- **Charger Input Voltage May Be Higher, Equal to or Lower Than Battery Voltage**
- Charges Any Number of Cells Up to 30V*
- 1% Voltage Accuracy for Rechargeable Lithium Batteries
- 100mV Current Sense Voltage for High Efficiency
- **Battery Can Be Directly Grounded**
- **500kHz Switching Frequency Minimizes Inductor Size**
- Charging Current Easily Programmable or Shut Down

APPLICATIONS

- Battery Charging of NiCd, NiMH, Lead-Acid or Lithium Rechargeable Cells
- Precision Current Limited Power Supply
- Constant-Voltage/Constant-Current Supply
- Transducer Excitation

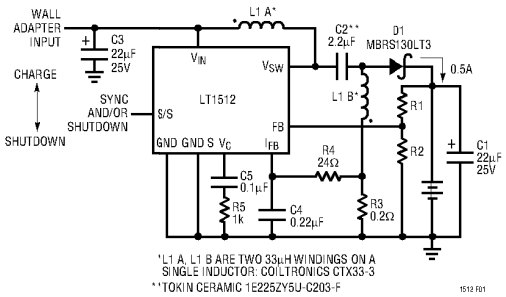
*Maximum Input Voltage = 40V – V_{BAT}

DESCRIPTION

The LT®1512 is a 500kHz current mode switching regulator specially configured to create a constant-current/ constant-voltage battery charger. In addition to the usual voltage feedback node, it has a current sense feedback circuit for accurately controlling output current of a flyback or SEPIC (Single-Ended Primary Inductance Converter) topology charger. These topologies allow the current sense circuit to be ground referred and completely separated from the battery itself, simplifying battery switching and system grounding problems. In addition, these topologies allow charging even when the input voltage is lower than the battery voltage.

Maximum switch current on the LT1512 is 1.5A. This allows battery charging currents up to 1A for a single lithium-ion cell. Accuracy of 1% in constant-voltage mode is perfect for lithium battery applications. Charging current can be easily programmed for all battery types.

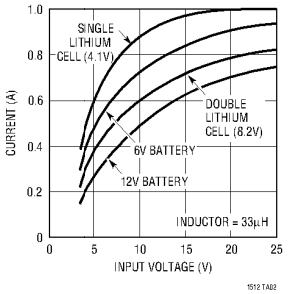
TYPICAL APPLICATION



*L1 A, L1 B ARE TWO 33µH WINDINGS ON A SINGLE INDUCTOR: COILTRONICS CTX33-3
**TOKIN CERAMIC 1E225ZY5U-C203-F

Figure 1. SEPIC Charger with 0.5A Output Current

Maximum Charging Current

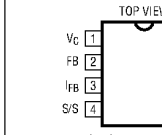


ACTUAL PROGRAMMED CHARGING CURRENT WILL BE INDEPENDENT OF INPUT VOLTAGE AND BATTERY VOLTAGE IF IT DOES NOT EXCEED THE VALUES SHOWN. THESE ARE ELECTRICAL LIMITATIONS BASED ON MAXIMUM SWITCH CURRENT. PACKAGE THERMAL LIMITATIONS MAY REDUCE MAXIMUM CHARGING CURRENT. SEE APPLICATIONS INFORMATION.

ABSOLUTE MAXIMUM RATINGS

Input Voltage 30V
Switch Voltage 40V
S/S Pin Voltage 30V
FB Pin Voltage (Transient, 10ms) ..... ±10V
V_{FB} Pin Current 10mA
I_{FB} Pin Voltage (Transient, 10ms) ..... ±10V
Storage Temperature Range ..... –65°C to 150°C
Ambient Temperature Range
  LT1512C (Note 3) ..... 0°C to 70°C
  LT1512I ..... –40°C to 85°C
Operating Junction Temperature Range
  LT1512C (Note 3) ..... –20°C to 125°C
  LT1512I ..... –40°C to 125°C
  Short Circuit ..... 0°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE 8-LEAD PDIP
S8 PACKAGE 8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 100°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 130°C/W (S)

NOTE: CONTACT FACTORY CONCERNING 16-LEAD FUSED-LEAD GN PACKAGE WITH LOWER THERMAL RESISTANCE

ORDER PART NUMBER
LT1512CN8 LT1512CS8 LT1512IN8 LT1512IS8
S8 PART MARKING
1512 1512I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_C = 0.6V, V_{FB} = V_{REF}, I_{FB} = 0V, V_{SW} and S/S pins open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	V_{FB} Reference Voltage	Measured at FB Pin V_C = 0.8V	 ●	1.233 1.228	1.245 1.245	1.257 1.262	V V
	FB Input Current	V_{FB} = V_{REF}	 ●		300	550 600	nA nA
	FB Reference Voltage Line Regulation	2.7V ≤ V_{IN} ≤ 25V, V_C = 0.8V	●		0.01	0.03	%/V
V_{IREF}	I_{FB} Reference Voltage	Measured at I_{FB} Pin V_{FB} = 0V, V_C = 0.8V	 ●	–107 –110	–100 –100	–93 –90	mV mV
	I_{FB} Input Current	V_{IFB} = V_{IREF} (Note 2)	●	10	25	35	µA
	I_{FB} Reference Voltage Line Regulation	2.7V ≤ V_{IN} ≤ 25V, V_C = 0.8V	●		0.01	0.05	%/V
g_m	Error Amplifier Transconductance	ΔI_C = ±25µA	 ●	1100 700	1500	1900 2300	µmho µmho
	Error Amplifier Source Current	V_{FB} = V_{REF} – 150mV, V_C = 1.5V	●	120	200	350	µA
	Error Amplifier Sink Current	V_{FB} = V_{REF} + 150mV, V_C = 1.5V	●		1400	2400	µA
	Error Amplifier Clamp Voltage	High Clamp, V_{FB} = 1V Low Clamp, V_{FB} = 1.5V		1.70 0.25	1.95 0.40	2.30 0.52	V V
A_V	Error Amplifier Voltage Gain				500		V/V
	V_C Pin Threshold	Duty Cycle = 0%		0.8	1	1.25	V
f	Switching Frequency	2.7V ≤ V_{IN} ≤ 25V 0°C ≤ T_J ≤ 125°C –40°C ≤ T_J < 0°C (LT1512I)	 ●	450 430 400	500 500	550 580 580	kHz kHz kHz
	Maximum Switch Duty Cycle		●	88	95		%
	Switch Current Limit Blanking Time				130	260	ns
BV	Output Switch Breakdown Voltage	0°C ≤ T_J ≤ 125°C –40°C ≤ T_J < 20°C (LT1512I)	●	40 35	47		V V

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_C = 0.6V, V_{FB} = V_{REF}, I_{FB} = 0V, V_{SW} and S/S pins open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{SAT}	Output Switch ON Resistance	I_{SW} = 2A	●		0.5	0.8	Ω
I_{LIM}	Switch Current Limit	Duty Cycle = 50%	●	1.5	1.9	2.7	A
		Duty Cycle = 80% (Note 1)	●	1.3	1.7	2.5	A
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch ON Time				15	25	mA/A
	Control Voltage to Switch Current Transconductance				2		A/V
	Minimum Input Voltage		●		2.4	2.7	V
I_Q	Supply Current	2.7V ≤ V_{IN} ≤ 25V	●		4	5.5	mA
	Shutdown Supply Current	2.7V ≤ V_{IN} ≤ 25V, $V_{S/S}$ ≤ 0.6V 0°C ≤ T_J ≤ 125°C −40°C ≤ T_J ≤ 0°C (LT1512I)	●		12	30 50	µA µA
	Shutdown Threshold	2.7V ≤ V_{IN} ≤ 25V	●	0.6	1.3	2	V
	Shutdown Delay		●	5	12	25	µs
	S/S Pin Input Current	0V ≤ $V_{S/S}$ ≤ 5V	●	−10		15	µA
	Synchronization Frequency Range		●	600		800	kHz

The ● denotes specifications which apply over the full operating temperature range.

Note 1: For duty cycles (DC) between 50% and 85%, minimum guaranteed switch current is given by I_{LIM} = 0.667 (2.75 – DC).

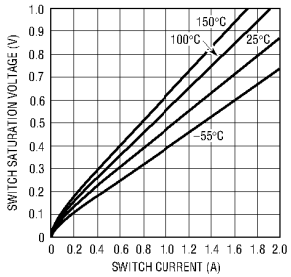
Note 2: The I_{FB} pin is servoed to its regulating state with V_C = 0.8V.

Note 3: Commercial devices are guaranteed over 0°C to 125°C junction temperature range and 0°C to 70°C ambient temperature range. These parts are also designed, characterized and expected to operate over the −20°C to 85°C extended ambient temperature range, but are not tested at −20°C or 85°C. Devices with full guaranteed electrical specifications over the ambient temperature range −40°C to 85°C are available as industrial parts with an "I" suffix.

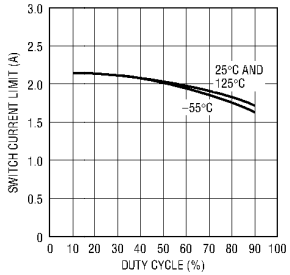
Maximum allowable ambient temperature may be limited by power dissipation. Parts may not necessarily be operated simultaneously at maximum power dissipation and maximum ambient temperature. Temperature rise calculations must be done as shown in the Applications Information section to ensure that maximum junction temperature does not exceed 125°C limit. With high power dissipation, maximum ambient temperature may be less than 70°C.

TYPICAL PERFORMANCE CHARACTERISTICS

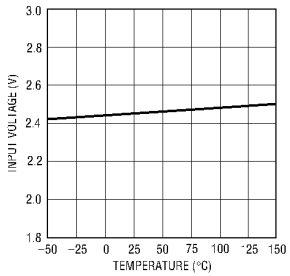
Switch Saturation Voltage vs Switch Current



Switch Current Limit vs Duty Cycle



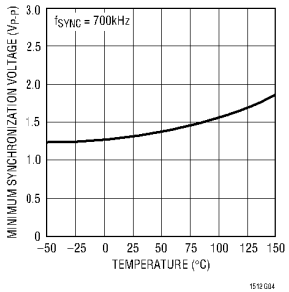
Minimum Input Voltage vs Temperature



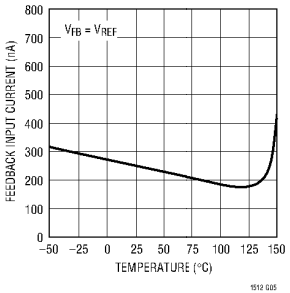
Tournez la page S.V.P.

TYPICAL PERFORMANCE CHARACTERISTICS

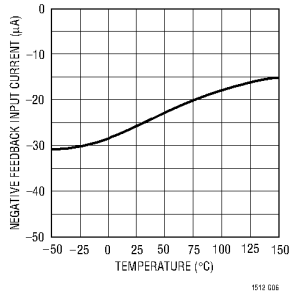
Minimum Peak-to-Peak Synchronization Voltage vs Temp



Feedback Input Current vs Temperature



Negative Feedback Input Current vs Temperature



PIN FUNCTIONS

V_C: The compensation pin is primarily used for frequency compensation, but it can also be used for soft starting and current limiting. It is the output of the error amplifier and the input of the current comparator. Peak switch current increases from 0A to 1.8A as the V_C voltage varies from 1V to 1.9V. Current out of the V_C pin is about 200µA when the pin is externally clamped below the internal 1.9V clamp level. Loop frequency compensation is performed with a capacitor or series RC network from the V_C pin *directly to the ground pin* (avoid ground loops).

FB: The feedback pin is used for positive output voltage sensing. This pin is the inverting input to the voltage error amplifier. The R1/R2 voltage divider connected to FB defines Li-Ion float voltage at full charge, or acts as a voltage limiter for NiCd or NiMH applications. Input bias current is typically 300nA, so divider current is normally set to 100µA to swamp out any output voltage errors due to bias current. The noninverting input of this amplifier is tied internally to a 1.245V reference. The grounded end of the output voltage divider should be connected directly to the LT1512 ground pin (avoid ground loops).

I_{FB}: The current feedback pin is used to sense charging current. It is the input to a current sense amplifier that controls charging current when the battery voltage is below the programmed voltage. During constant-current operation, the I_{FB} pin regulates at −100mV. Input resistance of this pin is 5kΩ, so filter resistance (R4, Figure 1) should be less than 50Ω. The 24Ω, 0.22µF filter shown in Figure 1 is used to convert the pulsating current in the sense resistor to a smooth DC current feedback signal.

S/S: This pin can be used for shutdown and/or synchronization. It is logic level compatible, but can be tied to V_{IN} if desired. It defaults to a high ON state when floated. A logic low state will shut down the charger to a micropower state. Driving the S/S pin with a continuous logic signal of 600kHz to 800kHz will synchronize switching frequency to the external signal. Shutdown is avoided in this mode with an internal timer.

V_{IN}: The input supply pin should be bypassed with a low ESR capacitor located right next to the IC chip. The grounded end of the capacitor must be connected directly to the ground plane to which the GND pin is connected.

GND S, GND: The LT1512 uses separate ground pins for switch current (GND) and the control circuitry (GND S). This isolates the control ground from any induced voltage created by fast switch currents. Both pins should be tied directly to the ground plane, but the external control circuit components such as the voltage divider, frequency compensation network and I_{FB} bypass capacitor should

PIN FUNCTIONS

be connected directly to the GND S pin or to the ground plane close to the point where the GND S pin is connected.

V_{SW}: The switch pin is the collector of the power switch, carrying up to 1.5A of current with fast rise and fall times. Keep the traces on this pin as short as possible to minimize radiation and voltage spikes. In particular, the path in Figure 1 which includes SW to C2, D1, C1 and around to the LT1512 ground pin should be as short as possible to minimize voltage spikes at switch turn-off.

BLOCK DIAGRAM

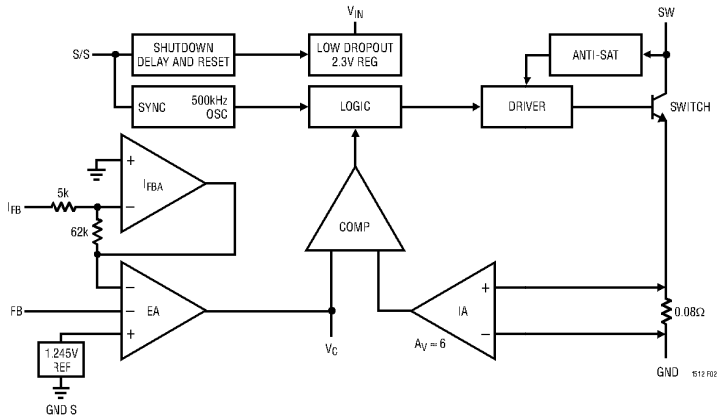


Figure 2

OPERATION

The LT1512 is a current mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage or current. Referring to the Block Diagram, the switch is turned "on" at the start of each oscillator cycle. It is turned "off" when switch current reaches a predetermined level. Control of output voltage and current is obtained by using the output of a dual feedback voltage sensing error amplifier to set switch current trip level. This technique has the advantage of simplified loop frequency compensation. A low dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1512. This low dropout design allows input voltage to vary from 2.7V to 25V. A 500kHz oscillator is the basic clock for all internal timing. It turns "on" the output switch via the logic and driver circuitry. Special adaptive antisat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A unique error amplifier design has two inverting inputs which allow for sensing both output voltage and current. A 1.245V bandgap reference biases the noninverting input. The first inverting input of the error amplifier is brought out for positive output voltage sensing. The second inverting input is driven by a "current" amplifier which is sensing output current via an external current sense resistor. The

OPERATION

current amplifier is set to a fixed gain of –12.5 which provides a –100mV current limit sense voltage.

The error signal developed at the amplifier output is brought out externally and is used for frequency compensation. During normal regulator operation this pin sits at a voltage between 1V (low output current) and 1.9V (high output current). Switch duty cycle goes to zero if the V_C pin is pulled below the V_C pin threshold, placing the LT1512 in an idle mode.

APPLICATIONS INFORMATION

The LT1512 is an IC battery charger chip specifically optimized to use the SEPIC converter topology. The SEPIC topology has unique advantages for battery charging. It will operate with input voltages above, equal to or below the battery voltage, has no path for battery discharge when turned off and eliminates the snubber losses of flyback designs. It also has a current sense point that is ground referred and need not be connected directly to the battery. The two inductors shown are actually just two identical windings on one inductor core, although two separate inductors can be used.

A current sense voltage is generated with respect to ground across R3 in Figure 1. The average current through R3 is always identical to the current delivered to the battery. The LT1512 current limit loop will servo the voltage across R3 to –100mV when the battery voltage is below the voltage limit set by the output divider R1/R2. Constant current charging is therefore set at 100mV/R3. R4 and C4 filter the current signal to deliver a smooth feedback voltage to the I_{FB} pin. R1 and R2 form a divider for battery voltage sensing and set the battery float voltage. The suggested value for R2 is 12.4k. R1 is calculated from:

$$R1 = \frac{R2(V_{BAT} - 1.245)}{1.245 + R2(0.3\mu A)}$$

V_{BAT} = battery float voltage
0.3μA = typical FB pin bias current

A value of 12.4k for R2 sets divider current at 100μA. This is a constant drain on the battery when power to the charger is off. If this drain is too high, R2 can be increased to 41.2k, reducing divider current to 30μA. This introduces an additional uncorrectable error to the constant voltage float mode of about ±0.5% as calculated by:

$$V_{BAT}\ \text{Error} = \frac{\pm 0.15\mu A(R1)(R2)}{1.245(R1+R2)}$$

±0.15μA = expected variation in FB bias current around the nominal 0.3μA typical value.

With R2 = 41.2k and R1 = 228k, (V_{BAT} = 8.2V), the error due to variations in bias current would be ±0.42%.

A second option is to disconnect the voltage divider with a small NMOS transistor as shown in Figure 3. To ensure adequate drive to the transistor (even when the V_{IN} voltage is at its lowest operating point of 2.4V), the FET gate is driven wth a peak detected voltage via D2. Note that there are two connections for D2. The L1 A connection must be used if the voltage divider is set for less than 3.5V (fully charged battery). Gate drive is equal to battery voltage *plus* input voltage. The disadvantage of this connection is that Q1 will still be "on" if the V_{IN} voltage is active and the charger is shut down via the S/S pin. The L1 B connection allows Q1 to turn off when V_{IN} is off or when shutdown is initiated, but the reduced gate drive (=V_{BAT}) is not adequate to ensure a Q1 on-state for fully charged battery voltages less than 3.5V. Do not substitute for Q1 unless the new device has adequate V_{GS} maximum rating, especially if D2 is connected to L1A. C6 filters the gate drive and R5 pulls the gate low when switching stops.

Disconnecting the divider leaves only D1 diode leakage as a battery drain. See Diode Selection for a discussion of diode leakage.

High Current Micropower Synchronous Buck-Boost DC/DC Converter

FEATURES

- **Regulated Output with Input Above, Below or Equal to the Output**
- **Single Inductor, No Schottky Diodes**
- **High Efficiency: Up to 95%**
- **25µA Quiescent Current in Burst Mode® Operation**
- **Up to 1.2A Continuous Output Current from a Single Lithium-Ion**
- **True Output Disconnect in Shutdown**
- 2.4V to 5.5V Input Range
- 2.4V to 5.25V Output Range
- 1MHz Fixed Frequency Operation
- Synchronizable Oscillator
- Selectable Burst Mode or Fixed Frequency Operation
- <1µA Quiescent Current in Shutdown
- Small, Thermally Enhanced 12-Lead (4mm × 3mm) DFN package

APPLICATIONS

- Handheld Computers
- Handheld Instruments
- MP3 Players
- Digital Cameras

LT, LTC and LT are registered trademarks of Linear Technology Corporation.
Burst Mode is a registered trademark of Linear Technology Corporation.

DESCRIPTION

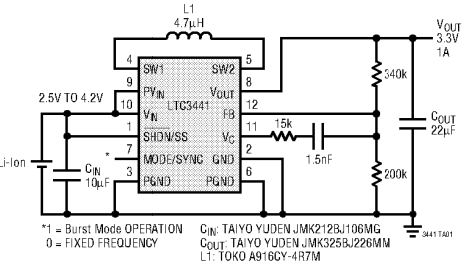
The LTC®3441 is a high efficiency, fixed frequency, buck-boost DC/DC converter that operates efficiently from input voltages above, below or equal to the output voltage. The topology incorporated in the IC provides a continuous transfer function through all operating modes, making the product ideal for single lithium ion or multicell applications where the output voltage is within the battery voltage range.

The device includes two 0.10Ω N-channel MOSFET switches and two 0.11Ω P-channel switches. External Schottky diodes are optional, and can be used for a moderate efficiency improvement. The operating frequency is internally set to 1MHz and can be synchronized up to 1.7MHz. Quiescent current is only 25µA in Burst Mode operation, maximizing battery life in portable applications. Burst Mode operation is user controlled and can be enabled by driving the MODE/SYNC pin high. If the MODE/SYNC pin is driven low or with a clock, then fixed frequency switching is enabled.

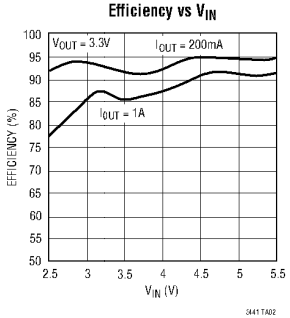
Other features include a 1µA shutdown, soft-start control, thermal shutdown and current limit. The LTC3441 is available in a thermally enhanced 12-lead (4mm × 3mm) DFN package.

TYPICAL APPLICATION

Li-Ion to 3.3V at 1A Buck-Boost Converter



Efficiency vs V_{IN}



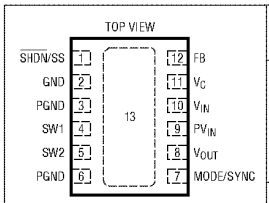
Tournez la page S.V.P.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, V_{OUT} Voltage ..... –0.3V to 6V
SW1, SW2 Voltage
DC ..... –0.3V to 6V
Pulsed < 100ns ..... –0.3V to 7V
SHDN/SS, MODE/SYNC Voltage ..... –0.3V to 6V
Operating Temperature Range (Note 2) .. –40°C to 85°C
Maximum Junction Temperature (Note 4) ..... 125°C
Storage Temperature Range ..... –65°C to 125°C

PACKAGE/ORDER INFORMATION



DE12 PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C
θ_{JA} = 53°C/W 1-LAYER BOARD
θ_{JA} = 43°C/W 4-LAYER BOARD
θ_{JC} = 4.3°C/W
EXPOSED PAD IS PGND (PIN 13)
MUST BE SOLDERED TO PCB

ORDER PART NUMBER
LTC3441EDE
DE PART MARKING
3441

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{OUT} = 3.6V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Start-Up Voltage		●		2.3	2.4	V
Output Voltage Adjust Range		●	2.4		5.25	V
Feedback Voltage		●	1.19	1.22	1.25	V
Feedback Input Current	V_{FB} = 1.22V			1	50	nA
Quiescent Current—Burst Mode Operation	V_C = 0V, MODE/SYNC = 3V (Note 3)			25	40	µA
Quiescent Current—SHDN	SHDN = 0V, Not Including Switch Leakage			0.1	1	µA
Quiescent Current—Active	MODE/SYNC = 0V (Note 3)			520	900	µA
NMOS Switch Leakage	Switches B and C			0.1	7	µA
PMOS Switch Leakage	Switches A and D			0.1	10	µA
NMOS Switch On Resistance	Switches B and C			0.10		Ω
PMOS Switch On Resistance	Switches A and D			0.11		Ω
Input Current Limit		●	2	3.2		A
Max Duty Cycle	Boost (% Switch C On) Buck (% Switch A In)	● ●	70 100	88		% %
Min Duty Cycle		●			0	%
Frequency Accuracy		●	0.85	1	1.15	MHz
MODE/SYNC Threshold		●	0.4		1.4	V
MODE/SYNC Input Current	$V_{MODE/SYNC}$ = 5.5V			0.01	1	µA
Error Amp AV_{OL}				90		dB
Error Amp Source Current				14		µA
Error Amp Sink Current				300		µA
SHDN/SS Threshold	When IC is Enabled	●	0.4	1	1.4	V
SHDN/SS Threshold	When EA is at Max Boost Duty Cycle			2	2.4	V
SHDN/SS Input Current	V_{SHDN} = 5.5V			0.01	1	µA

ELECTRICAL CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

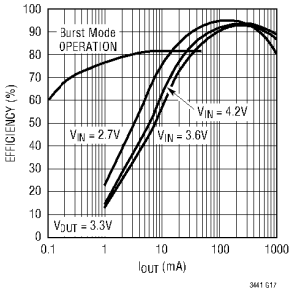
Note 2: The LTC3441E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Current measurements are preformed when the outputs are not switching.

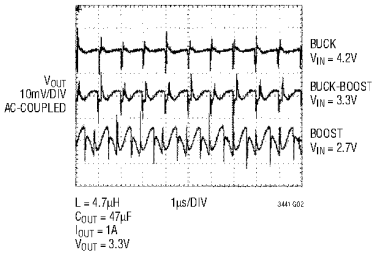
Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

TYPICAL PERFORMANCE CHARACTERISTICS

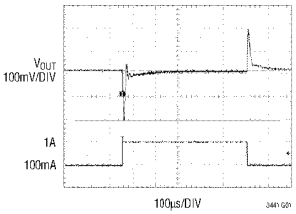
Efficiency



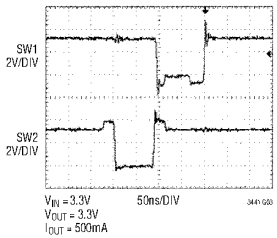
V_{OUT} Ripple at 1A Load



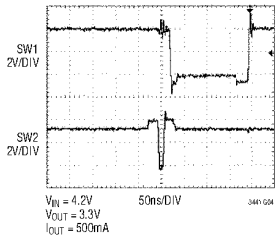
Load Transient Response, 100mA to 1A



Switch Pins in Buck-Boost Mode

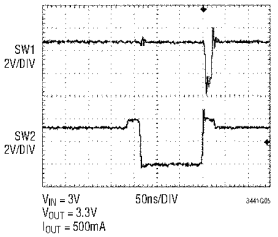


Switch Pins Entering Buck-Boost Mode

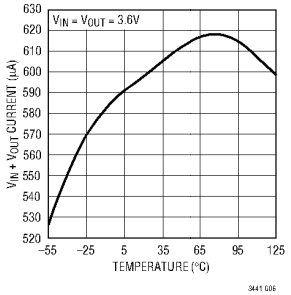


TYPICAL PERFORMANCE CHARACTERISTICS

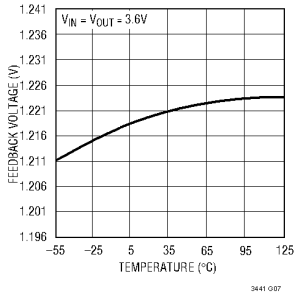
Switch Pins Before Entering Boost Mode



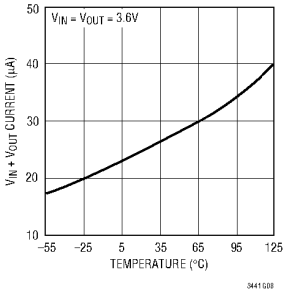
Active Quiescent Current



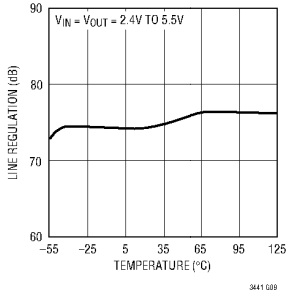
Feedback Voltage



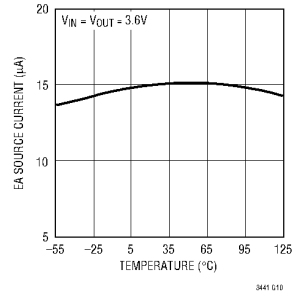
Burst Mode Quiescent Current



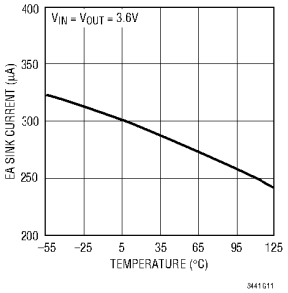
Feedback Voltage Line Regulation



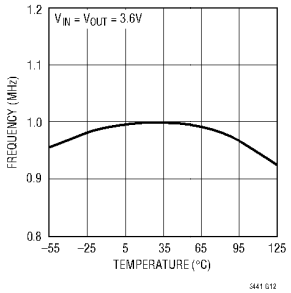
Error Amp Source Current



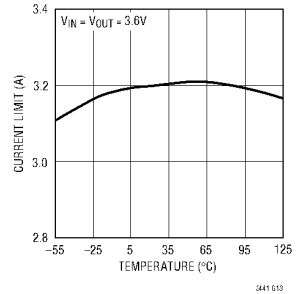
Error Amp Sink Current



Output Frequency

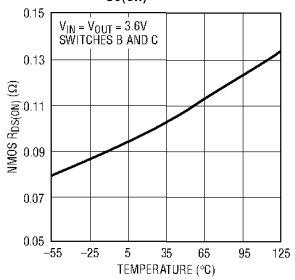


Current Limit

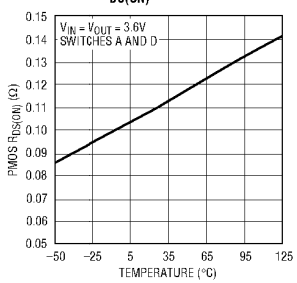


TYPICAL PERFORMANCE CHARACTERISTICS

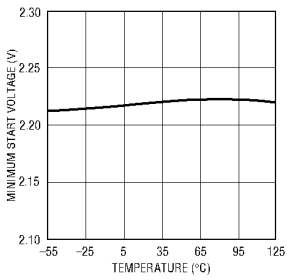
NMOS $R_{DS(ON)}$



PMOS $R_{DS(ON)}$



Minimum Start Voltage



PIN FUNCTIONS

$\overline{SHDN}$/SS (Pin 1): Combined Soft-Start and Shutdown. Applied voltage < 0.4V shuts down the IC. Tie to >1.4V to enable the IC and >2.4V to ensure the error amp is not clamped from soft-start. An RC from the shutdown command signal to this pin will provide a soft-start function by limiting the rise time of the V_C pin.

GND (Pin 2): Signal Ground for the IC.

PGND (Pins 3, 6, 13 Exposed Pad): Power Ground for the Internal NMOS Power Switches

SW1 (Pin 4): Switch pin where the internal switches A and B are connected. Connect inductor from SW1 to SW2. An optional Schottky diode can be connected from this SW1 to ground. Minimize trace length to keep EMI down.

SW2 (Pin 5): Switch pin where the internal switches C and D are connected. An optional Schottky diode can be connected from SW2 to V_{OUT} (it is required where V_{OUT} > 4.3V). Minimize trace length to keep EMI down.

MODE/SYNC (Pin 7): Burst Mode Select and Oscillator Synchronization.

MODE/SYNC = High: Enable Burst Mode Operation. During the period where the IC is supplying energy to the output, the inductor peak inductor current will reach 0.8A and return to zero current on each cycle. In Burst Mode operation the operation is variable frequency, which provides a significant efficiency improvement at light loads. The Burst Mode operation will continue until the pin is driven low.

MODE/SYNC = Low: Disable Burst Mode operation and maintain low noise, constant frequency operation .

MODE/SYNC = External CLK : Synchronization of the internal oscillator and Burst Mode operation disable. A clock pulse width between 100ns and 2µs and a clock frequency between 2.3MHz and 3.4MHz (twice the desired frequency) is required to synchronize the IC.

$$f_{OSC} = f_{SYNC}/2$$

V_{OUT} (Pin 8): Output of the Synchronous Rectifier. A filter capacitor is placed from V_{OUT} to GND. A ceramic bypass capacitor is recommended as close to the V_{OUT} and GND pins as possible.

PV_{IN} (Pin 9): Power V_{IN} Supply Pin. A 10µF ceramic capacitor is recommended as close to the PV_{IN} and PGND pins as possible

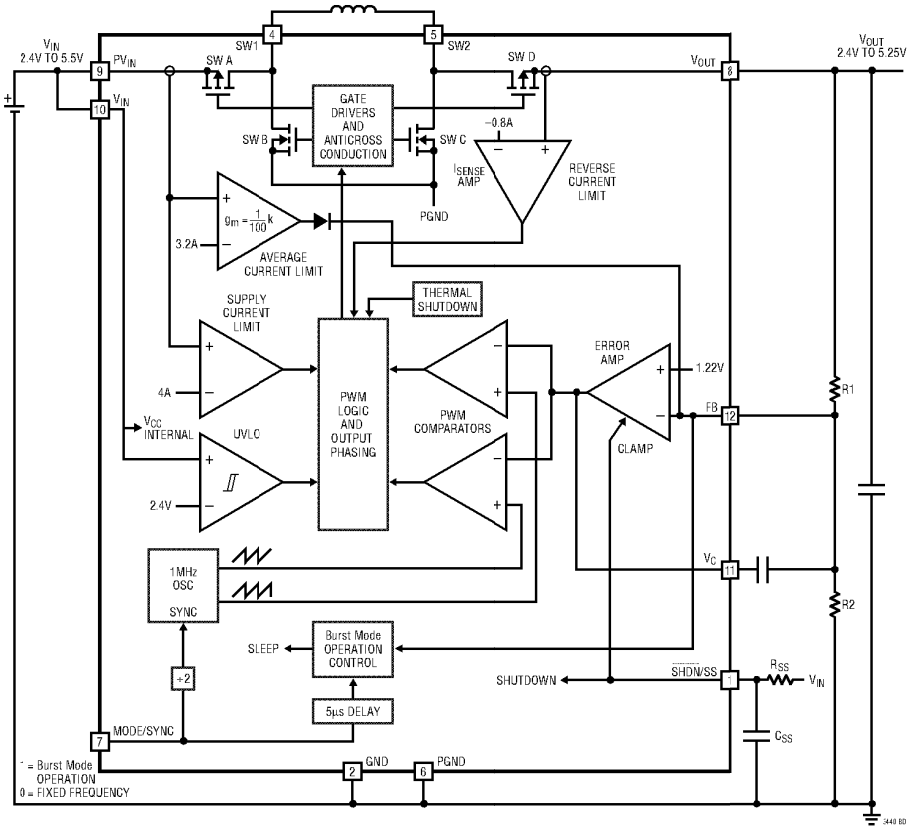
V_{IN} (Pin 10): Input Supply Pin. Internal V_{CC} for the IC.

V_C (Pin 11): Error Amp Output. A frequency compensation network is connected from this pin to the FB pin to compensate the loop. See the section "Compensating the Feedback Loop" for guidelines.

FB (Pin 12): Feedback Pin. Connect resistor divider tap here. The output voltage can be adjusted from 2.4V to 5.25V. The feedback reference voltage is typically 1.22V.

Tournez la page S.V.P.

BLOCK DIAGRAM



OPERATION

The LTC3441 provides high efficiency, low noise power for applications such as portable instrumentation. The LTC proprietary topology allows input voltages above, below or equal to the output voltage by properly phasing the output switches. The error amp output voltage on the V_C pin determines the output duty cycle of the switches. Since the V_C pin is a filtered signal, it provides rejection of frequencies from well below the switching frequency. The low $R_{DS(ON)}$, low gate charge synchronous switches provide high frequency pulse width modulation control at high efficiency. Schottky diodes across the synchronous switch D and synchronous switch B are not required, but provide a lower drop during the break-before-make time (typically 15ns). The addition of the Schottky diodes will improve peak efficiency by typically 1% to 2%. High efficiency is achieved at light loads when Burst Mode operation is entered and when the IC's quiescent current is a low 25µA.

LOW NOISE FIXED FREQUENCY OPERATION

Oscillator

The frequency of operation is factory trimmed to 1MHz. The oscillator can be synchronized with an external clock applied to the MODE/SYNC pin. A clock frequency of twice the desired switching frequency and with a pulse width of at least 100ns is applied. The oscillator sync range is 1.15MHz to 1.7MHz (2.3MHz to 3.4MHz sync frequency).

Error Amp

The error amplifier is a voltage mode amplifier. The loop compensation components are configured around the amplifier to obtain stability of the converter. The SHDN/SS pin will clamp the error amp output, V_C, to provide a soft-start function.

Supply Current Limit

The current limit amplifier will shut PMOS switch A off once the current exceeds 4A typical. Before the switch current limit, the average current limit amp (3.2A typical) will source current into the FB pin to drop the output voltage. The current amplifier delay to output is typically 50ns.

Reverse Current Limit

The reverse current limit amplifier monitors the inductor current from the output through switch D. Once a negative inductor current exceeds –800mA typical, the IC will shut off switch D.

Output Switch Control

Figure 1 shows a simplified diagram of how the four internal switches are connected to the inductor, V_{IN}, V_{OUT} and GND. Figure 2 shows the regions of operation for the LTC3441 as a function of the internal control voltage, V_{CI}. The V_{CI} voltage is a level shifted voltage from the output of the error amp (V_C pin) (see Figure 5). The output switches are properly phased so the transfer between operation modes is continuous, filtered and transparent to the user. When V_{IN} approaches V_{OUT} the Buck/Boost region is reached where the conduction time of the four switch region is typically 150ns. Referring to Figures 1 and 2, the various regions of operation will now be described.

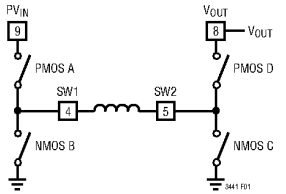


Figure 1. Simplified Diagram of Output Switches

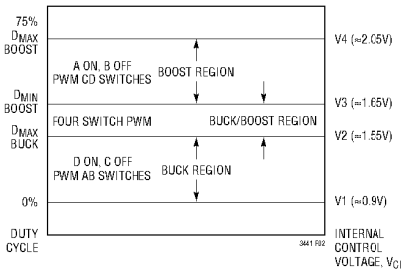


Figure 2. Switch Control vs Internal Control Voltage, V_{CI}

OPERATION

Buck Region ($V_{IN} > V_{OUT}$)

Switch D is always on and switch C is always off during this mode. When the internal control voltage, V_{CI}, is above voltage V1, output A begins to switch. During the off time of switch A, synchronous switch B turns on for the remainder of the time. Switches A and B will alternate similar to a typical synchronous buck regulator. As the control voltage increases, the duty cycle of switch A increases until the maximum duty cycle of the converter in Buck mode reaches D_{MAX_BUCK}, given by:

$$D_{MAX\_BUCK} = 100 - D4_{SW}\ \%$$

where $D4_{SW}$ = duty cycle % of the four switch range.

$$D4_{SW} = (150ns \bullet f) \bullet 100\ \%$$

where f = operating frequency, Hz.

Beyond this point the "four switch," or Buck/Boost region is reached.

Buck/Boost or Four Switch ($V_{IN} \sim V_{OUT}$)

When the internal control voltage, V_{CI}, is above voltage V2, switch pair AD remain on for duty cycle D_{MAX_BUCK}, and the switch pair AC begins to phase in. As switch pair AC phases in, switch pair BD phases out accordingly. When the V_{CI} voltage reaches the edge of the Buck/Boost range, at voltage V3, the AC switch pair completely phase out the BD pair, and the boost phase begins at duty cycle $D4_{SW}$.

The input voltage, V_{IN}, where the four switch region begins is given by:

$$V_{IN} = \frac{V_{OUT}}{1-(150ns \bullet f)} V$$

The point at which the four switch region ends is given by:

$$V_{IN} = V_{OUT}(1 - D) = V_{OUT}(1 - 150ns \bullet f)\ V$$

Boost Region ($V_{IN} < V_{OUT}$)

Switch A is always on and switch B is always off during this mode. When the internal control voltage, V_{CI}, is above voltage V3, switch pair CD will alternately switch to provide a boosted output voltage. This operation is typical to a synchronous boost regulator. The maximum duty cycle of the converter is limited to 88% typical and is reached when V_{CI} is above V4.

Burst Mode OPERATION

Burst Mode operation is when the IC delivers energy to the output until it is regulated and then goes into a sleep mode where the outputs are off and the IC is consuming only 25µA. In this mode the output ripple has a variable frequency component that depends upon load current.

During the period where the device is delivering energy to the output, the peak current will be equal to 800mA typical and the inductor current will terminate at zero current for each cycle. In this mode the typical maximum average output current is given by:

$$I_{OUT(MAX)BURST} \approx \frac{0.2 \bullet V_{IN}}{V_{OUT} + V_{IN}} A$$

Burst Mode operation is user controlled, by driving the MODE/SYNC pin high to enable and low to disable.

The peak efficiency during Burst Mode operation is less than the peak efficiency during fixed frequency because the part enters full-time 4-switch mode (when servicing the output) with discontinuous inductor current as illustrated in Figures 3 and 4. During Burst Mode operation, the control loop is nonlinear and cannot utilize the control voltage from the error amp to determine the control mode, therefore full-time 4-switch mode is required to maintain the Buck/Boost function. The efficiency below 1mA becomes dominated primarily by the quiescent current and not the peak efficiency. The equation is given by:

$$\text{Efficiency Burst} \approx \frac{(\eta bm) \bullet I_{LOAD}}{25\mu A + I_{LOAD}}$$

where (ηbm) is typically 75% during Burst Mode operation.

OPERATION

Burst Mode Operation to Fixed Frequency Transient Response

When transitioning from Burst Mode operation to fixed frequency, the system exhibits a transient since the modes of operation have changed. For most systems this transient is acceptable, but the application may have stringent input current and/or output voltage requirements that dictate a broad-band voltage loop to minimize the transient. Lowering the DC gain of the loop will facilitate the task (5M from FB to V_C) at the expense of DC load regulation. Type 3 compensation is also recommended to broad band the loop and roll off past the two pole response of the LC of the converter (see Closing the Feedback Loop).

SOFT-START

The soft-start function is combined with shutdown. When the SHDN/SS pin is brought above typically 1V, the IC is enabled but the EA duty cycle is clamped from the V_C pin. A detailed diagram of this function is shown in Figure 5. The components R_{SS} and C_{SS} provide a slow ramping voltage on the SHDN/SS pin to provide a soft-start function.

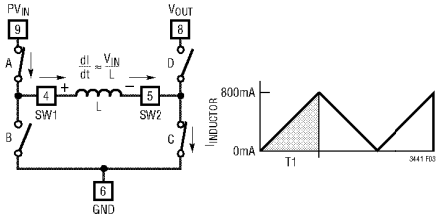


Figure 3. Inductor Charge Cycle During Burst Mode Operation

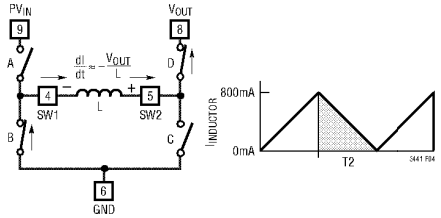


Figure 4. Inductor Discharge Cycle During Burst Mode Operation

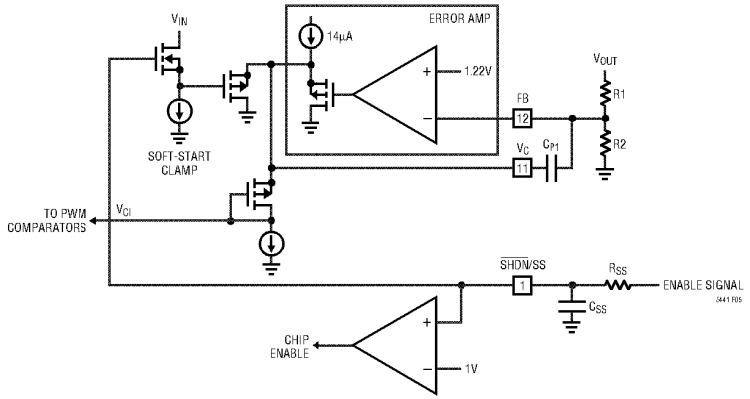


Figure 5. Soft-Start Circuitry

Tournez la page S.V.P.

APPLICATIONS INFORMATION

COMPONENT SELECTION

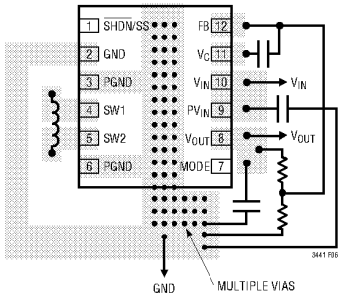


Figure 6. Recommended Component Placement. Traces Carrying High Current are Direct. Trace Area at FB and V_C Pins are Kept Low. Lead Length to Battery Should be Kept Short. V_{OUT} and V_{IN} Ceramic Capacitors Close to the IC Pins

Inductor Selection

The high frequency operation of the LTC3441 allows the use of small surface mount inductors. The inductor current ripple is typically set to 20% to 40% of the maximum inductor current. For a given ripple the inductance terms are given as follows:

$$L > \frac{V_{IN(MIN)}^2 \bullet (V_{OUT} - V_{IN(MIN)}) \bullet 100}{f \bullet I_{OUT(MAX)} \bullet \%Ripple \bullet V_{OUT}^2}\ H,$$

$$L > \frac{V_{OUT} \bullet (V_{IN(MAX)} - V_{OUT}) \bullet 100}{f \bullet I_{OUT(MAX)} \bullet \%Ripple \bullet V_{IN(MAX)}}\ H$$

where f = operating frequency, Hz

%Ripple = allowable inductor current ripple, %

$V_{IN(MIN)}$ = minimum input voltage, V

$V_{IN(MAX)}$ = maximum input voltage, V

V_{OUT} = output voltage, V

$I_{OUT(MAX)}$ = maximum output load current

For high efficiency, choose an inductor with a high frequency core material, such as ferrite, to reduce core loses. The inductor should have low ESR (equivalent series resistance) to reduce the I^2R losses, and must be able to handle the peak inductor current without saturating. Molded chokes or chip inductors usually do not have enough core to support the peak inductor currents in the 1A to 2A region. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor. See Table 1 for suggested components and Table 2 for a list of component suppliers.

Table 1. Inductor Vendor Information

SUPPLIER	PHONE	FAX	WEB SITE
Coilcraft	(847) 639-6400	(847) 639-1469	www.coilcraft.com
Coiltronics	(561) 241-7876	(561) 241-9339	www.coiltronics.com
Murata	USA: (814) 237-1431 (800) 831-9172	USA: (814) 238-0490	www.murata.com
Sumida	USA: (847) 956-0666 Japan: 81(3) 3607-5111	(847) 956-0702 81(3) 3607-5144	www.japanlink.com/sumida

Output Capacitor Selection

The bulk value of the capacitor is set to reduce the ripple due to charge into the capacitor each cycle. The steady state ripple due to charge is given by:

$$\%Ripple\_Boost = \frac{I_{OUT(MAX)} \bullet (V_{OUT} - V_{IN(MIN)}) \bullet 100}{C_{OUT} \bullet V_{OUT}^2 \bullet f}\%$$

$$\%Ripple\_Buck = \frac{I_{OUT(MAX)} \bullet (V_{IN(MAX)} - V_{OUT}) \bullet 100}{C_{OUT} \bullet V_{IN(MAX)} \bullet V_{OUT} \bullet f}\%$$

where C_{OUT} = output filter capacitor, F

The output capacitance is usually many times larger in order to handle the transient response of the converter. For a rule of thumb, the ratio of the operating frequency to the unity-gain bandwidth of the converter is the amount the output capacitance will have to increase from the above calculations in order to maintain the desired transient response.

The other component of ripple is due to the ESR (equivalent series resistance) of the output capacitor. Low ESR capacitors should be used to minimize output voltage ripple. For surface mount applications, Taiyo Yuden ceramic capacitors, AVX TPS series tantalum capacitors or Sanyo POSCAP are recommended.

APPLICATIONS INFORMATION

Input Capacitor Selection

Since the V_{IN} pin is the supply voltage for the IC it is recommended to place at least a 4.7µF, low ESR bypass capacitor.

Table 2. Capacitor Vendor Information

SUPPLIER	PHONE	FAX	WEB SITE
AVX	(803) 448-9411	(803) 448-1943	www.avxcorp.com
Sanyo	(619) 661-6322	(619) 661-1055	www.sanyovideo.com
Taiyo Yuden	(408) 573-4150	(408) 573-4159	www.t-yuden.com

Optional Schottky Diodes

The Schottky diodes across the synchronous switches B and D are not required (V_{OUT} < 4.3V), but provide a lower drop during the break-before-make time (typically 15ns) of the NMOS to PMOS transition, improving efficiency. Use a Schottky diode such as an MBRM120T3 or equivalent. Do not use ordinary rectifier diodes, since the slow recovery times will compromise efficiency. For applications with an output voltage above 4.3V, a Schottky diode is required from SW2 to V_{OUT}.

Output Voltage < 2.4V

The LTC3441 can operate as a buck converter with output voltages as low as 0.4V. The part is specified at 2.4V minimum to allow operation without the requirement of a Schottky diode. Synchronous switch D is powered from V_{OUT} and the $R_{DS(ON)}$ will increase at low output voltages, therefore a Schottky diode is required from SW2 to V_{OUT} to provide the conduction path to the output.

Output Voltage > 4.3V

A Schottky diode from SW to V_{OUT} is required for output voltages over 4.3V. The diode must be located as close to the pins as possible in order to reduce the peak voltage on SW2 due to the parasitic lead and trace inductance.

Input Voltage > 4.5V

For applications with input voltages above 4.5V which could exhibit an overload or short-circuit condition, a 2Ω/1nF series snubber is required between the SW1 pin and GND. A Schottky diode from SW1 to V_{IN} should also be added as close to the pins as possible. For the higher input voltages, V_{IN} bypassing becomes more critical; therefore, a ceramic bypass capacitor as close to the V_{IN} and GND pins as possible is also required.

Operating Frequency Selection

Additional quiescent current due to the output switches GATE charge is given by:

Buck: $800e^{-12} \bullet V_N \bullet f$

Boost: $400e^{-12} \bullet (V_{IN} + V_{OUT}) \bullet f$

Buck/Boost: $f \bullet (1200e^{-12} \bullet V_{IN} + 400e^{-12} \bullet V_{OUT})$

where f = switching frequency

Closing the Feedback Loop

The LTC3441 incorporates voltage mode PWM control. The control to output gain varies with operation region (Buck, Boost, Buck/Boost), but is usually no greater than 15. The output filter exhibits a double pole response is given by:

$$f_{FILTER\_POLE} = \frac{1}{2 \bullet \pi \bullet \sqrt{L \bullet C_{OUT}}} Hz$$

where C_{OUT} is the output filter capacitor.

The output filter zero is given by:

$$f_{FILTER\_ZERO} = \frac{1}{2 \bullet \pi \bullet R_{ESR} \bullet C_{OUT}} Hz$$

where R_{ESR} is the capacitor equivalent series resistance.

A troublesome feature in Boost mode is the right-half plane zero (RHP), and is given by:

$$f_{RHPZ} = \frac{V_{IN}^2}{2 \bullet \pi \bullet I_{OUT} \bullet L \bullet V_{OUT}} Hz$$

The loop gain is typically rolled off before the RHP zero frequency.

A simple Type I compensation network can be incorporated to stabilize the loop but at a cost of reduced bandwidth and slower transient response. To ensure proper phase margin, the loop requires to be crossed over a decade before the LC double pole.

APPLICATIONS INFORMATION

The unity-gain frequency of the error amplifier with the Type I compensation is given by:

$$f_{UG} = \frac{1}{2 \bullet \pi \bullet R1 \bullet CP1} Hz$$

Most applications demand an improved transient response to allow a smaller output filter capacitor. To achieve a higher bandwidth, Type III compensation is required. Two zeros are required to compensate for the double-pole response.

$$f_{POLE1} \approx \frac{1}{2 \bullet \pi \bullet 32e^3 \bullet R1 \bullet C_{P1}} Hz$$

Which is extremely close to DC

$$f_{ZERO1} = \frac{1}{2 \bullet \pi \bullet R_Z \bullet C_{P1}} Hz$$

$$f_{ZERO2} = \frac{1}{2 \bullet \pi \bullet R1 \bullet C_{Z1}} Hz$$

$$f_{POLE2} = \frac{1}{2 \bullet \pi \bullet R_Z \bullet C_{P2}} Hz$$

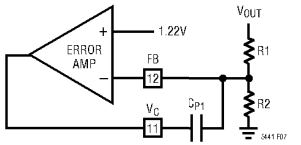


Figure 7. Error Amplifier with Type I Compensation

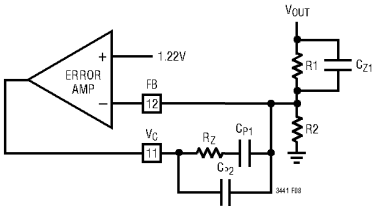
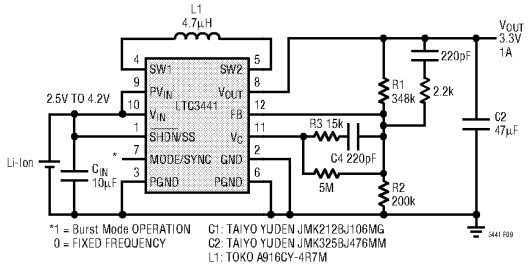


Figure 8. Error Amplifier with Type III Compensation



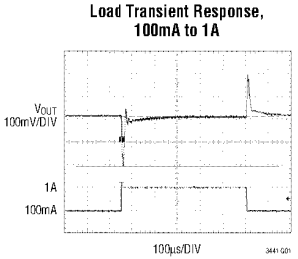


Figure 9. Fast Transient Response Compensation for Step Load or Mode Change

Features

- Carrier Frequency f_{osc} 100 kHz - 150 kHz
- Typical Data Rate up to 5 kbaud at 125 kHz
- Suitable for Manchester and Bi-phase Modulation
- Power Supply from the Car Battery or from 5-V Regulated Voltage
- Optimized for Car Immobilizer Applications
- Tuning Capability
- Microcontroller-compatible Interface
- Low Power Consumption in Standby Mode
- Power-supply Output for Microcontroller

Applications

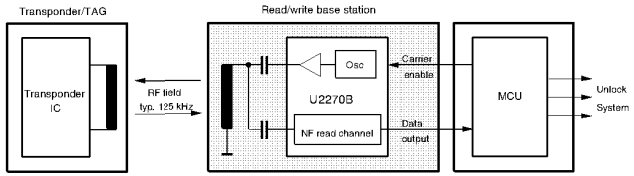
- Car Immobilizers
- Animal Identification
- Access Control
- Process Control

Description

The U2270B is an IC for IDIC® read/write base stations in contactless identification and immobilizer systems.

The IC incorporates the energy-transfer circuit to supply the transponder. It consists of an on-chip power supply, an oscillator and a coil driver optimized for automotive-specific distances. It also includes all signal-processing circuits which are necessary to transform the small input signal into a microcontroller-compatible signal.

System Block Diagram



Tournez la page S.V.P.

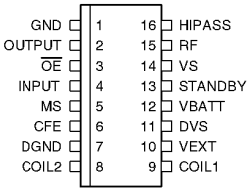
Read/Write Base Station

U2270B

Rev. 4684A–RFID–02/03

Pin Configuration

Figure 1. Pinning



Pin Description

Pin	Symbol	Function
1	GND	Ground
2	OUTPUT	Data output
3	$\overline{OE}$	Data output enable
4	INPUT	Data input
5	MS	Mode select coil 1: common mode/differential mode
6	CFE	Carrier frequency enable
7	DGND	Driver ground
8	COIL2	Coil driver 2
9	COIL1	Coil driver 1
10	VEXT	External power supply
11	DVS	Driver supply voltage
12	VBatt	Battery voltage
13	STANDBY	Standby input
14	VS	Internal power supply (5 V)
15	RF	Frequency adjustment
16	HIFASS	DC decoupling