**ELECTRICAL CHARACTERISTICS**

The ■ denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25^\circ C$.

### Symbol Parameter

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</table>

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<td>$\mu A$</td>
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**TYPICAL PERFORMANCE CHARACTERISTICS**

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

**Note 2:** The LT1308AAG, LT1308ACT, LT1308BCS, and LT1308BCF are designed, characterized and expected to meet the industrial temperature limits, but are not tested at $-40^\circ C$ and $85^\circ C$. Individual devices are guaranteed over the $-40^\circ C$ to $85^\circ C$ operating temperature range.

**Note 3:** Bias current flows into FB pin.

**Note 4:** Switch current limit guaranteed by design and/or correlation to static tests. Duty cycle affects current limit due to rising generator (see Bodo Diagram).

**Note 5:** Bias current flows out of LBO pin.

**Note 6:** Connect the four GPIO pins (Pins 4-7) together at the device. Similarly, connect the three SW pins (Pins 9-13) together and the two VIN pins (Pins 11, 12) together at the device.
TYPICAL PERFORMANCE CHARACTERISTICS

PIN FUNCTIONS

SC-8 Package

VCC (Pin 1): Compensation Pin for Error Amplifier. Connect a series RC from this pin to ground. Typical values are 47kΩ and 100pF. Minimize trace area at Vcc.

FB (Pin 2): Feedback Pin. Reference voltage is 1.22V. Connect resistive divider tap here. Minimize trace area at FB. Set VOUT according to: VOUT = 1.22V(1 + R1/R2).

SHDN (Pin 3): Shutdown. Ground this pin to turn off switcher. To enable, tie to 1V or more. SHDN does not need to be at VBB to enable the device.

GND (Pin 4): Ground. Connect directly to local ground plane. Ground plane should encompass all components associated with the LT1308. PCB copper connected to Pin 4 also functions as a heat sink. Maximize this area to keep chip heating to a minimum.

SW (Pin 5): Switch Pin. Connect inductor/diode here. Minimize trace area at this pin to keep EMI down.

VBB (Pin 6): Supply Pin. Must have local bypass capacitor right at the pin, connected directly to ground.

LBI (Pin 7): Low-Battery Detector Input. 200mV reference. Voltage on LBI must stay between ~100mV and 1V. Low-battery detector does not function with SHDN pin grounded. Float LBI pin if not used.

LBO (Pin 8): Low-Battery Detector Output. Open collector, can sink 50mA. A 220kΩ pull-up is recommended. LBO is high impedance when SHDN is grounded.

TSSOP Package

VCC (Pin 1): Compensation Pin for Error Amplifier. Connect a series RC from this pin to ground. Typical values are 47kΩ and 100pF. Minimize trace area at Vcc.

FB (Pin 2): Feedback Pin. Reference voltage is 1.22V. Connect resistive divider tap here. Minimize trace area at FB. Set VOUT according to: VOUT = 1.22V(1 + R1/R2).

SHDN (Pin 3): Shutdown. Ground this pin to turn off switcher. To enable, tie to 1V or more. SHDN does not need to be at VBB to enable the device.

GND (Pins 4, 5, 6, 7): Ground. Connect directly to local ground plane. Ground plane should encompass all components associated with the LT1308. PCB copper connected to these pins also functions as a heat sink. Connect all pins to ground copper to get the best heat transfer. This keeps chip heating to a minimum.

SW (Pins 8, 9, 10): Switch Pins. Connect inductor/diode here. Minimize trace area at these pins to keep EMI down. Connect all SW pins together at the package.

VBB (Pins 11, 12): Supply Pins. Must have local bypass capacitor right at the pins, connected directly to ground. Connect both VBB pins together at the package.

LBI (Pin 13): Low-Battery Detector Input. 200mV reference. Voltage on LBI must stay between ~100mV and 1V. Low-battery detector does not function with SHDN pin grounded. Float LBI pin if not used.

LBO (Pin 14): Low-Battery Detector Output. Open collector, can sink 50mA. A 220kΩ pull-up is recommended. LBO is high impedance when SHDN is grounded.
**APPLICATIONS INFORMATION**

**OPERATION**

The LT1308A combines a current mode, fixed frequency PWM architecture with Burst Mode micro power operation to maintain high efficiency at light loads. Operation can be best understood by referring to the block diagram in Figure 2. J1 and Q2 form a bandgap reference core whose loop is closed around the output of the converter. When $V_{IN}$ is 1V, the feedback voltage of 1.22V, along with an 80mV drop across R5 and R6, forward biases Q1 and Q2's base collector junctions to 300mV. Because this is not enough to saturate either transistor, FB can be at a higher voltage than $V_{IN}$. When there is no load, FB rises slightly above 1.22V, causing $V_C$ (the error amplifier's output) to decrease. When $V_C$ reaches the bias voltage on hysteric comparator A1, A1's output goes low, turning off all circuitry except the input stage, error amplifier and low-battery detector. Total current consumption in this state is 143μA. As output loading causes the FB voltage to decrease, A1's output goes high, enabling the rest of the IC. Switch current is limited to approximately 400mA initially after A1's output goes high. If the load is light, the output voltage (and FB voltage) will increase until A1's output goes low, turning off the rest of the LT1308A. Low frequency ripple voltage appears at the output. The ripple frequency is dependent on load current and output capacitance. This Burst Mode operation keeps the output regulated and reduces average current into the IC, resulting in high efficiency even at load currents of 1mA or less.

If the output load increases sufficiently, A1's output remains high, resulting in continuous operation. When the LT1308A is running continuously, peak switch current is controlled by $V_C$ to regulate the output voltage. The switch is turned on at the beginning of each switch cycle. When the summation of a signal representing switch current and a ramp generator (introduced to avoid subharmonic oscillations at duty factors greater than 50%) exceeds the $V_C$ signal, comparator A2 changes state, resetting the flip-flop and turning off the switch. Output voltage increases as switch current is increased. The output, attenuated by a resistor divider, appears at the FB pin, closing the overall loop. Frequency compensation is provided by an external series RC network connected between the $V_C$ pin and ground.

Low-battery detector A4's open-collector output (LB0) pulls low when the LB0 pin voltage drops below 200mV. There is no hysteresis in A4, allowing it to be used as an amplifier in some applications. The entire device is disabled when the SHDN pin is brought low. To enable the converter, SHDN must be at 1V or greater. It need not be tied to $V_{IN}$ as on the LT1308B.

The LT1308B differs from the LT1308A in that there is no hysteresis in comparator A1. Also, the bias point on A1 is set lower than on the LT1308B so that switching can occur at inductor current less than 100mA. Because A1 has no hysteresis, there is no Burst Mode operation at light loads and the device continues switching at constant frequency. This results in the absence of low frequency output voltage ripple at the expense of efficiency.

The difference between the two devices is clearly illustrated in Figure 3. The top two tracings in Figure 3 shows an LT1308A/LT1308B circuit, using the components indicated in Figure 1, set to a 5V output. Input voltage is 3V. Load current is stepped from 50mA to 500mA for both circuits. Low frequency Burst Mode operation voltage ripple is observed on Trace A, while none is observed on Trace B.

At light loads, the LT1308B will begin to skip alternate cycles. The load point at which this occurs can be decreased by increasing the inductor value. However, output ripple will continue to be significantly less than on the LT1308B output ripple. Further, the LT1308B can be forced into micro power mode, where $I_L$ falls from 3mA to 200μA by sinking 40μA or more of the $V_C$ pin. This stops switching by causing A1's output to go low.

Figure 3. LT1308A Exhibits Burst Mode Operation Output Voltage Ripple at 50mA Load, LT1308B Does Not
APPLICATIONS INFORMATION

Waveforms for a LT1308B 5V to 12V boost converter using a 1μF ceramic output capacitor are pictured in Figures 4 and 5. In Figure 4, the converter is operating in continuous mode, delivering a load current of approximately 500mA. The top trace is the output. The voltage increases as inductor current is dumped into the output capacitor during the switch off time, and the voltage decrease when the switch is on. Ripple voltage is in this case due to capacitance, as the ceramic capacitor has little ESR. The middle trace is the switch voltage. This voltage alternates between VCESAT and VOUT plus the diode drop. The lower trace is the switch current. At the beginning of the switch cycle, the current is 1.2A. At the end of the switch on time, the current has increased to 2A, at which point the switch turns off and the inductor current flows into the output capacitor through the diode. Figure 5 depicts converter waveforms at a light load. Here the converter operates in discontinuous mode. The inductor current reaches zero during the switch off time, resulting in some ringing at the switch node. The ringing frequency is set by switch capacitance, diode capacitance and inductance. This ringing has little energy, and its sinuous shape suggests it is free from harmonics. Minimizing the copper area at the switch node will prevent this from causing interference problems.

LAYOUT HINTS

The LT1308A/LT1308B switch current at high speed, mandating careful attention to layout for proper performance. You will not get advertised performance with careless layout. Figure 6 shows recommended component placement for an SO-8 package boost (step-up) converter. Follow this closely in your PC layout. Note the direct path of the switching loops. Input capacitor C1 must be placed close (<5mm) to the IC package. As little as 10mm of wire or PC trace from C1 to VOUT will cause problems such as inability to regulate or oscillation.

The negative terminal of output capacitor C2 should be close to the ground pin(s) of the LT1308A/LT1308B. Doing this reduces dI/dt in the ground copper which keeps high frequency spikes to a minimum. The DC/DC converter ground should tie to the PC board ground plane at one place only, to avoid introducing dI/dt in the ground plane.

Figure 5. Converter Waveforms in Continuous Mode.

Figure 4. 5V to 12V Boost Converter Waveforms in Continuous Mode. 1μF Ceramic Capacitor Used at Output

A SEPIC (Single-Ended Primary Inductance Converter) schematic is shown in Figure 8. This converter topology produces a regulated output over an input voltage range that spans (i.e., can be higher or lower than) the output. Recommended component placement for an SO-8 package SEPIC is shown in Figure 9.

Figure 7. Recommended Component Placement for TSSOP Boost Converter. Placement is Similar to Figure 4.

Figure 6. Recommended Component Placement for SO-8 Package Boost Converter. Note Direct High Current Paths Using Wide PC Traces. Minimize Trace Area at Pin 1 (VOUT) and Pin 2 (FB). Use Multiple Vias to Tie Pin 4 Copper to Ground Plane. Use Vias at One Location Only to Avoid Introducing Switching Currents into the Ground Plane.

Figure 8. SEPIC (Single-Ended Primary Inductance Converter) Converts 3V to 16V Input to a 3V/500mA Regulated Output

Figure 9. Recommended Component Placement for SEPIC

Figure 7 shows recommended component placement for a boost converter using the TSSOP package. Placement is similar to the SO-8 package layout.
**APPLICATIONS INFORMATION**

**SHDN PIN**

The LT1308A/LT1308B SHDN pin is improved over the LT1308. The pin does not require tying to V\textsubscript{CC} to enable the device, but needs only a logic level signal. The voltage on the SHDN pin can vary from 1V to 10V independent of V\textsubscript{CC}. Further, floating this pin has the same effect as grounding, which is to shut the device down, reducing current drain to 1μA or less.

**LOW-BATTERY DETECTOR**

The low-battery detector on the LT1308A/LT1308B features improved accuracy and drive capability compared to the LT1308. The 200mV reference has an accuracy of ±2% and the open-collector output can sink 50μA. The LT1308A/LT1308B low-battery detector is a simple PNP input gain stage with an open-collector NPN output. The negative input of the gain stage is tied internally to a 230mV reference. The positive input is the LBI pin. Arrangement as a low-battery detector is straightforward. Figure 10 details hookup. R1 and R2 need only be low enough in value so that the bias current of the LBI pin doesn't cause large errors. For R2, 100k is adequate. The 200mV reference can also be accessed as shown in Figure 11.

**START-UP**

The LT1308A/LT1308B can start up into heavy loads, unlike many CMOS DC/DC converters that derive operating voltage from the output (a technique known as "bootstrapping"). Figure 13 details start-up waveforms of Figure 1's circuit with a 20Ω load and V\textsubscript{IN} of 1.5V. Inductor current rises to 3.5A as the output capacitor is charged. After the output reaches 5V, inductor current is about 1A.

In Figure 14, the loads 50Ω and input voltage is 3V. Output voltage reaches 5V in 500μs after the device is enabled. Figure 15 shows start-up behavior of Figure 5's SEPIC circuit, driven from a 9V input with a 10Ω load. The output reaches 5V in about 1ms after the device is enabled.

**5V Boost Converter of Figure 1. Start-up from 1.5V Input into 20Ω Load**

**5V SEPIC Start-up from 9V Input into 10Ω Load**

**Soft-Start**

In some cases it may be undesirable for the LT1308A/LT1308B to operate at current limit during start-up, e.g., when operating from a battery composed of alkaline cells. The inrush current may cause sufficient internal voltage drop to trigger a low-battery indicator. A programmable soft-start can be implemented with 4 discrete components. A 5V to 12V boost converter using the LT1308B is detailed in Figure 16. C4 differentiates V\textsubscript{OUT}, causing a current to flow into R3 as V\textsubscript{OUT} increases. When this current exceeds 0.7V/33k, or 21μA, current flows into the base of Q1. Q1's collector then pulls current out of the V\textsubscript{CC} pin, creating a feedback loop where the slope of V\textsubscript{OUT} is limited as follows:

$$\frac{\Delta V_{OUT}}{\Delta t} = 0.7V \cdot 33k \cdot C4$$

With C4 = 33μF, V\textsubscript{OUT} is limited to 640mW/μs. Start-up waveforms for Figure 16's circuit are pictured in Figure 17. Without the soft-start circuit implemented, the inrush current reaches 3A. The circuit reaches final output voltage in approximately 250μs. Adding the soft-start components reduces inductor current to less than 1A, as detailed in Figure 18, while the time required to reach final output voltage increases to about 15ms. C4 can be adjusted to achieve any output slew rate desired.
so that copper loss is minimized. Acceptable inductance values range between 2μH and 20μH, with 4.7μH best for most applications. Lower value inductors are physically smaller than higher value inductors for the same current capability.

Table 1 lists some inductors we have found to perform well in LT1308A/LT1308B application circuits. This is not an exclusive list.

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Capacitors

Equivalent Series Resistance (ESR) is the main issue regarding selection of capacitors, especially the output capacitors.

The output capacitors specified for use with the LT1308A/LT1308B circuits have low ESR and are specifically designed for power supply applications. Output voltage ripple of a boost converter is equal to ESR multiplied by switch current. The performance of the AVX TPS2227VM06 220μF tantalum can be evaluated by referring to Figure 3.

Figure 20 shows load step response of a 50mA to 500mA load using a 47μF tantalum capacitor at the output. Without the phase lead capacitor, there is some ringing, suggesting the phase margin is low. C2 is then added, and response to the same load step is pictured in Figure 21. Some phase margin is restored, improving the response. Next, C2 is replaced by a 10μF, X5R dielectric, ceramic capacitor.

Without C2, load step response is pictured in Figure 22.

Although the output settles faster than the tantalum case, there is appreciable ringing, again suggesting phase margin is low. Figure 23 depicts load step response using the 10μF ceramic output capacitor and C2. Response is clear and no ringing is evident. Ceramic capacitors have the added benefit of lowering ripple at the switching frequency due to their very low ESR. By applying C2 in tandem with the series RC at the Vx pin, loop response can be tailored to optimize response using ceramic output capacitors.

Figure 19. 5V to 12V Boost Converter

Figure 20. Load Step Response of LT1308B 5V to 12V Boost Converter with 47μF Tantalum Output Capacitor

Figure 21. Load Step Response with 47μF Tantalum Output Capacitor and Phase Lead Capacitor C2

Figure 22. Load Step Response with 10μF X5R Ceramic Output Capacitor
LT1512
SEPIC Constant-Current/
Constant-Voltage
Battery Charger

FEATURES
• Charger Input Voltage May Be Higher, Equal to or Lower Than Battery Voltage
• Charges Any Number of Cells Up to 30V*
• 1% Voltage Accuracy for Rechargeable Lithium Batteries
• 100mV Current Sense Voltage for High Efficiency
• Battery Can Be Directly Grounded
• 500kHz Switching Frequency Minimizes
  Inductor Size
• Charging Current Easily Programmable or Shut Down

APPLICATIONS
• Battery Charging of NiCd, NiMH, Lead-Acid
  or Lithium Rechargeable Cells
• Precision Current Limited Power Supply
• Constant-Voltage/Constant-Current Supply
• Transducer Excitation

DESCRIPTION
The LT1512 is a 500kHz current mode switching regula-
tor specially configured to create a constant-current/
constant-voltage battery charger. In addition to the usual
voltage feedback node, it has a current sense feedback
circuit for accurately controlling output current of a flyback
or SEPIC (Single-Ended Primary Inductance Converter)
topology charger. These topologies allow the current
sense circuit to be grounded referred and completely sepa-
rated from the battery itself, simplifying battery switching
and system grounding problems. In addition, these topolo-
gies allow charging even when the input voltage is lower
than the battery voltage.

Maximum switch current on the LT1512 is 1.5A. This
allows battery charging currents up to 1A for a single
lithium-ion cell. Accuracy of 1% in constant-voltage mode
is perfect for lithium battery applications. Charging cur-
cent can be easily programmed for all battery types.

Maximum Charging Current

![Diagram of charging current] (Figure 1. SEPIC Charger with 9.5A Output Current)

ELECTRICAL CHARACTERISTICS

\[ V_{in} = 3V, \, V_{c} = 0.6V, \, V_{ref} = 20V, \, I_{ch} = 4V, \, V_{SW} \text{ and } I_{SW} \text{ pins open, unless otherwise noted.} \]

<table>
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<td>( V_{o} )</td>
<td>Output Voltage</td>
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<td>( I_{in} )</td>
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<td>( I_{out} )</td>
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**TYPICAL APPLICATION**

![Diagram of typical application] (Diagram added)

**PACKAGE/ORDER INFORMATION**

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*Note: Input Voltage = VIN - VREF

**Figure 1. SEPIC Charger with 9.5A Output Current**
ELECTRICAL CHARACTERISTICS

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<td>Switch Current Limit</td>
<td>Duty Cycle = 50%</td>
<td>1.5</td>
<td>1.9</td>
<td>2.7</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Duty Cycle = 80% (Note 1)</td>
<td>1.3</td>
<td>1.7</td>
<td>2.5</td>
<td>A</td>
</tr>
<tr>
<td>IDISCH</td>
<td>Supply Current Increase During Switch On Time</td>
<td>15</td>
<td>25</td>
<td>mA</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Control Voltage to Switch Current</td>
<td>2</td>
<td>A/V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Transconductance</td>
<td>2.4</td>
<td>2.7</td>
<td>A/V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_S</td>
<td>Minimum Input Voltage</td>
<td>4</td>
<td>5.5</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Shutdown Current</td>
<td>2.4 V ≤ V_S ≤ 2.1 V</td>
<td>4</td>
<td>5.5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Shutdown Threshold</td>
<td>2.4 V ≤ V_S ≤ 2.1 V</td>
<td>0.6</td>
<td>1.2</td>
<td>2</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Shutdown Delay</td>
<td>5</td>
<td>12</td>
<td>25</td>
<td>μs</td>
<td></td>
</tr>
<tr>
<td>VDD</td>
<td>S/VS Pin Input Voltage</td>
<td>8 V ≤ V_S ≤ 5 V</td>
<td>10</td>
<td>15</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Synchronization Frequency Range</td>
<td>600</td>
<td>800</td>
<td>kHz</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The 1 indicates devices which apply over the full operating temperature range.

Note 1: For duty cycles (DC) between 50% and 85%, minimum guaranteed switch current is given by I_CSN = 0.67 (2.73 - DC).

Note 2: The VDD pin is not used except for the regulating state with VDD = 3.6 V.

Note 3: Synchronization devices are guaranteed over 0°C to 125°C junction temperature range and 0°C to 70°C ambient temperature range. These parts are also designed, characterized, and expected to operate over the -55°C to 85°C extended ambient temperature range, and are not tested at -50°C or 85°C. Devices with full guaranteed electrical specifications over the ambient temperature range -40°C to 85°C are available as industrial parts with a "I" suffix.

The 1 indicates devices which apply over the full operating temperature range.

Maximum allowable ambient temperature may be limited by power dissipation. Parts may not necessarily be operated simultaneously a maximum power dissipation and maximum ambient temperature.

Temperature rise calculations must be done as shown in the Applications Information section to ensure that maximum junction temperature does not exceed 125°C. With high power dissipation, maximum ambient temperature may be less than 70°C.

TYPICAL PERFORMANCE CHARACTERISTICS

Pin Functions

Vg The compensation pin is primarily used for frequency compensation; it can also be used for soft starting and current limiting. It is the output of the error amplifier and the input of the current comparator. Peak switch current increases from 0 A to 1.8 A as the Vg voltage varies from 0 V to 3 V. Current out of the Vg pin is about 200 μA when the pin is externally clamped below the internal 1.9 V clamp level. Loop frequency compensation is performed by a capacitor or series RC network from the Vg pin directly to the ground pin (avoid ground loops).

FB The feedback pin is used for positive output voltage sensing. This pin is the inverting input to the voltage error amplifier. The R1/R2 voltage divider connected to FB defines Li-Ion float voltage at full charge, or acts as a voltage limiter for NiCd or NiMH applications. Input bias current is typically 100 μA, so divider current is normally set to 100 μA to swap out any output voltage errors due to bias current. The noninverting input of this amplifier is tied internally to a 1.2545 V reference. The grounded end of the output voltage divider should be connected directly to the LT1512 ground pin (avoid ground loops).

Ig The current feedback pin is used to sense charging current. It is the input to a current sense amplifier that controls charging current when the battery voltage is below the programmed voltage. During constant current operation, the Ig pin regulates at -100 mA. Input resistance of this pin is 5 kΩ, so filter resistance (R4, Figure 1) should be less than 50 kΩ. The 240 kΩ 0.22 nF filter shown in Figure 1 is used to convert the pulsating current in the sense resistor to a smooth DC current feedback signal.

S/VS This pin can be used for shutdown and/or synchronization. It is logic level compatible, but can be tied to Vg if desired. It defaults to a high state when floated. A logic low state will shut down the charge to a microprocessor state. Driving the S/VS pin with a continuous logic signal of 60 kHz to 800 kHz will synchronize switching frequency to the external signal. Shutdown is avoided in this mode with an external timer.

Vg The input supply pin should be bypassed with a low ESR capacitor located right next to the IC chip. The grounded end of the capacitor must be connected directly to the ground plane to which the GND pin is connected.

GND S, GND O: The LT1512 uses separate ground pins for switch current (GND) and the control circuitry (GND S). This isolates the control ground from any induced voltage created by fast switch currents. Both pins should be tied directly to the ground plane, but the external control circuit components such as the voltage divider, frequency compensation network and Ig bypass capacitor should
PIN FUNCTIONS
be connected directly to the GND S pin or to the ground plane close to the point where the GND S pin is connected. VSW: The switch pin is the collector of the power switch, carrying up to 1.5A at current with fast rise and fall times. Keep the traces on this pin as short as possible to minimize radiation and voltage spikes. In particular, the path in Figure 1 which includes SW to Q2, Q1, C1 and around to the LT1512 ground pin should be as short as possible to minimize voltage spikes at switch turn-off.

LT1512

OPERATION
current amplifier is set to a fixed gain of -12.5 which provides a ~100mV current limit sense voltage. The error signal developed at the amplifier output is brought out externally and is used for frequency compensation. During normal regulator operation this pin sits at a voltage between 1V (low output current) and 1.9V (high output current). Switch duty cycle goes to zero if the Vc pin is pulled below the Vc pin threshold, placing the LT1512 in an idle mode.

APPLICATIONS INFORMATION
The LT1512 is an IC battery charger chip specifically optimized to use the SEPIC converter topology. The SEPIC topology has unique advantages for battery charging. It will operate with input voltages above, equal to or below the battery voltage, has no path for battery discharge when turned off and eliminates the snubber losses of flyback designs. It also has a current sense point that is ground referenced and need not be connected directly to the battery. The two inductors shown are actually just two identical windings on one inductor core, although two separate inductors can be used.

A current sense voltage is generated with respect to ground across R3 in Figure 1. The average current through R3 is always identical to the current delivered to the battery. The LT1512R current limit loop will sense the voltage across R3 to 100mV when the battery voltage is below the voltage limit set by the output divider R1/R2. Constant current charging therefore sets at 100mV/R3. R4 and C4 filter the current signal to deliver a smooth feedback voltage to the VFB pin. R1 and R2 form a divider for battery voltage sensing and set the battery float voltage. The suggested value for R2 is 12.4k. R1 is calculated from:

\[ R1 = \frac{VFB}{1.245} = \frac{2.45}{1.245} + \frac{2.45}{3.6uA} \]

VFB = battery float voltage
0.36uA = typical FB pin bias current

A value of 12.4k for R2 sets divider current at 100uA. This is a constant drain on the battery when power to the charger is off. If this drain is too high, R2 can be increased to 41.2k, reducing divider current to 30uA. This introduces an additional uncorrectable error to the constant voltage float mode of about 0.5% as calculated by:

\[ \frac{V_{FB}}{V_{REF}} = \frac{0.15uA \times (R1/R2)}{1.245 \times (R1/R2)} \]

0.15uA = expected variation in FB bias current around the nominal 0.36uA typical value.

With R2 = 41.2k and R1 = 228k (VFB = 8.2V), the error due to variations in bias current would be 0.42%.

A second option is to disconnect the voltage divider with a small NMOS transistor as shown in Figure 3. To ensure adequate drive to the transistor (even when the Vc voltage is at its lowest operating point of 2.4V), the gate is driven with a peak detected voltage via D2. Note that there are two connections for D2. The L1A connection must be used if the voltage divider is set for less than 5.5V (fully charged battery). Gate drive is equal to battery voltage plus input voltage. The disadvantage of this connection is that Q1 will still be on if the Vc voltage is active and the charger is shut down via the S/S pin. The L1B connection allows Q1 to turn off when Vc or if when shutdown is initiated, but the reduced gate drive (VFBt) is not adequate to ensure a Q1 on-state for fully charged battery voltages less than 5.5V. Do not substitute for Q1 unless the new device has adequate Vg maximum rating, especially if D2 is connected to L1A. G3 filters the gate drive and R6 pulls the gate low when switching stops. Disconnecting the divider leaves only DIODE leakage as a battery drain. See Diode Selection for a discussion of diode leakage.
FEATURES

- Regulated Output with Input Above, Below or Equal to the Output
- Single Inductor, No Schottky Diodes
- High Efficiency: 80 to 95%
- 25μA Quiescent Current in Burst Mode® Operation
- Up to 1.2A Continuous Output Current from a Single Lithium-Ion
- True Output Disconnect in Shutdown
- 2.4V to 5.5V Input Range
- 2.4V to 5.25V Output Range
- 1MHz Fixed Frequency Operation
- Synchronized Oscillator
- Selectable Burst Mode or Fixed Frequency Operation
- <1μA Quiescent Current in Shutdown
- Small, Thermally Enhanced 12-Lead (4mm x 3mm) DFN package

APPLICATIONS

- Handheld Computers
- Handheld Instruments
- MP3 Players
- Digital Cameras

DESCRIPTION

The LTC3441 is a high efficiency, fixed frequency, buck-boost DC/DC converter that operates efficiently from input voltages above, below or equal to the output voltage. The topology incorporates an internal current mode buck-boost converter, providing continuous output current to a synchronous rectification of the output voltage. The integrated circuit (IC) provides a continuous transfer function through various operating modes, allowing the product to be ideal for low power, battery-powered applications. The device includes two 0.1Ω N-channel MOSFET switches and two 0.1Ω P-channel switches. Internal Schottky diodes are optional, and can be used for a moderate efficiency improvement. The operating frequency is internally set to 1MHz and can be synchronized to 1.7MHz. Quiescent current is only 25μA in Burst Mode operation, minimizing battery requirements in portable applications. Burst Mode operation is user controlled and can be enabled by driving the MODE/SYNC pin high. If both the MODE/SYNC pin is driven low or with a clock, then fixed frequency switching is enabled.

Other features include a 1μA shutdown, soft-start control, interval output current limit. The LTC3441 is available in a thermally enhanced 12-lead (4mm x 3mm) DFN package.

TYPICAL APPLICATION

Li-ion to 5V at 1A Buck-Boost Converter

ELECTRICAL CHARACTERISTICS

The table and graph provided below are for reference only. Consult the LTC3441 datasheet for complete specifications and operating conditions.
ELECTRICAL CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC3441 is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the −40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Current measurements are performed when the outputs are not switching.

TYPICAL PERFORMANCE CHARACTERISTICS

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.
PIN FUNCTIONS

SHDN/SS (Pin 1): Combined Soft-Start and Shutdown. Applied voltage < 0.4V shuts down the IC. Tie to >1.4V to enable the IC and >2.4V to ensure the error amp is not clamped from soft-start. An RC from the shutdown command signal to this pin will provide a soft-start function by limiting the rise-time of the Vcc pin.

GND (Pin 2): Signal Ground for the IC.


SW1 (Pin 4): Switch pin where the internal switches A and B are connected. Connect inductor from SW1 to SW2. An optional Schottky diode can be connected from SW1 to ground. Minimize trace length to keep EMI down.

SW2 (Pin 5): Switch pin where the internal switches C and D are connected. An optional Schottky diode can be connected from SW2 to SW4. It is required where VOUT > 4.3V. Minimize trace length to keep EMI down.

MODE/SYNC (Pin 7): Burst Mode Select and Oscillator Synchronization.

MODE/SYNC = High: Enable Burst Mode Operation. During the period where the IC is supplying energy to the output, the inductor peak inductor current will reach 0.8A and return to zero current on each cycle. In Burst Mode operation the operation is variable frequency, which provides a significant efficiency improvement at light loads. The Burst Mode operation will continue until the pin is driven low.

MODE/SYNC = Low: Disable Burst Mode operation and maintain low noise, constant frequency operation.

MODE/SYNC = External CLK: Synchronization of the internal oscillator and Burst Mode operation is possible. A clock pulse width between 100ns and 2us and a clock frequency between 2.3MHz and 3.4MHz (twice the desired frequency) is required to synchronize the IC.

\[ f_{OSC} = \frac{f_{CLK}}{2} \]

VOUT (Pin 8): Output of the Synchronous Rectifier. A filter capacitor is placed from VOUT to GND. A ceramic bypass capacitor is recommended close to the VOUT and GND pins as possible.

PVIN (Pin 9): Power Supply Pin. A 10μF ceramic capacitor is recommended close to the PVIN and PGNE pins as possible.

VH (Pin 10): Input Supply Pin. Internal Vcc for the IC.

VC (Pin 11): Error Amp Output. A frequency compensation network is connected from this pin to the F3 pin to compensate the loop. See the section "Compensating the Feedback Loop" for guidelines.

FB (Pin 12): Feedback Pin. Connect resistor divider tap here. The output voltage can be adjusted from 2.2V to 5.25V. The feedback reference voltage is typically 1.22V.
OPERATION

The LTC3441 provides high efficiency, low noise power for applications such as portable instrumentation. The LTC proprietary typology allows input voltages above, below or equal to the output voltage by properly phasing the output switches. The error amp output voltage on the VC pin determines the output duty cycle of the switches. Since the VC pin is a filtered signal, it provides rejection of frequencies from well below the switching frequency. The low RDSON, low gate charge synchronous switches provide high frequency pulse width modulation control at high efficiency. Schottky diodes across the synchronous switch D and synchronous switch B are not required, but provide a lower drop during the break before make time (typically 15ns). The addition of the Schottky diodes will improve peak efficiency by typically 1% to 2%. High efficiency is achieved at light loads when Burst Mode operation is entered and when the IC’s quiescent current is a low 25μA.

LOW NOISE FIXED FREQUENCY OPERATION

Oscillator

The frequency of operation is factory trimmed to 1MHz. The oscillator can be synchronized with an external clock applied to the MODE/SYNC pin. A clock frequency off the desired switching frequency and with a pulse width of at least 100ns is applied. The oscillator sync range is 1.15MHz to 1.7MHz (2.3MHz to 3.4MHz sync frequency).

Error Amp

The error amplifier is a voltage mode amplifier. The loop compensation components are configured around the amplifier to obtain stability of the converter. The SHDN/SS pin will clamp the error amp output, VO, to provide a soft-start function.

Supply Current Limit

The current limit amplifier will shut PMOS switch A off once the current exceeds 4A typical. Before the switch current limit, the average current limit amp (3.2A typical) will source current into the FB pin to drop the output voltage. The current amplifier delay to output is typically 50ns.

Reverse Current Limit

The reverse current limit amplifier monitors the inductor current from the output through switch D. Once the negative inductor current exceeds -800mA typical, the IC will shut off switch D.

Output Switch Control

Figure 1 shows a simplified diagram of how the four internal switches are connected to the inductor, VIN, VOUT and GND. Figure 2 shows the regions of operation for the LTC3441 as a function of the internal control voltage, VCC. The VCC voltage is a level shifted voltage from the output of the error amp (VC pin) (see Figure 5). The output switches are properly phased so the transfer between operation modes is continuous, filtered and transparent to the user. When VCC approaches VOUT the Buck/Boost region is reached where the conduction time of the four switch region is typically 15ns. Referring to Figures 1 and 2, the various regions of operation will now be described.

Buck Region (VIN > VOUT)

Switch D is always on and switch C is always off during this mode. When the internal control voltage, VCC, is above voltage V1, output A begins to switch. During the off time of switch A, synchronous switch B turns on for the remainder of the time. Switches A and B will alternate similar to a typical synchronous buck regulator. As the control voltage increases, the cut off cycle of switch A increases until the maximum duty cycle of the converter in Buck mode reaches \( D_{MAX, BUCK} \) given by:

\[
D_{MAX, BUCK} = 100 - \frac{D_{SW}}{D_{SW} \times 100}
\]

where \( D_{SW} \) is duty cycle % of the four switch range.

\[
D_{SW} = \left( \frac{150ns \times f}{100} \right)
\]

where \( f \) is operating frequency, Hz.

Beyond this point the "four switch" or Buck/Boost region is reached.

Buck/Boost or Four Switch (VIN = VOUT)

When the internal control voltage, VCC, is above voltage V2, switch pair AD remain on for duty cycle \( D_{MAX, BUCK} \) and the switch pair AC begins to phase in. As switch pair AC phases in, switch pair BD phases out accordingly. When the VCC voltage reaches the edge of the Buck/Boost range, at voltage V3, the AC switch pair completely phase out the BD pair, and the boost phase begins at duty cycle \( D_{SW} \).

The input voltage, VIN, where the four switch region begins is given by:

\[
V_{IN} = \frac{V_{OUT} - V}{1 - 750ns \times f}
\]

The point at which the four switch region ends is given by:

\[
V_{IN} = V_{OUT}(1 - D) = V_{OUT}(1 - 750ns \times f)
\]

Efficiency Boost Region (VIN < VOUT)

Switch A is always on and switch B is always off during this mode. When the internal control voltage, VCC, is above voltage V3, switch pair CD will alternately switch to provide a boosted output voltage. This operation is typical to a synchronous boost regulator. The maximum duty cycle of the converter is limited to 88% typical and is reached when VCC is above V4.

Burst Mode OPERATION

Burst Mode operation is when the IC delivers energy to the output until it is regulated and then goes into a sleep mode where the outputs are off and the IC is consuming only 25μA. In this mode the output ripple has a variable frequency component that depends upon load current. During the period where the device is delivering energy to the output, the peak current will be equal to 800mA typical and the inductor current will terminate at zero current for each cycle. In this mode the typical maximum average output current is given by:

\[
I_{OUT/MAX,BURST} = \frac{0.2 \times V_{IN} - A}{V_{OUT} + V_{IN}}
\]

Burst Mode operation is user controlled by driving the MODE/SYNC pin high to enable and low to disable. The peak efficiency during Burst Mode operation is less than the peak efficiency during fixed frequency because the part enters full-time 4-switch mode when servicing the output with discontinuous inductor current as illustrated in Figures 3 and 4. During Burst Mode operation, the control loop is nonlinear and cannot utilize the control voltage from the error amp to control the control mode, therefore full-time 4-switch mode is required to maintain the Buck/Boost function. The efficiency below 1mA becomes dominated primarily by the quiescent current and not the peak efficiency. The equation is given by:

\[
\text{Efficiency Boost} = \frac{(\eta B) \times I_{LOAD}}{25μA + I_{LOAD}}
\]

where \( (\eta B) \) is typically 75% during Burst Mode operation.
**OPERATION**

**Burst Mode Operation to Fixed Frequency Transient Response**

When transitioning from Burst Mode operation to fixed frequency, the system exhibits a transient since the modes of operation have changed. For most systems this transient is acceptable, but the application may have stringent input current and/or output voltage requirements that dictate a broad-band voltage loop to minimize the transient. Lowering the IC gain of the loop will facilitate the task (SM from FB to V_{O}) at the expense of DC load regulation. Type S compensation is also recommended to broaden the loop and roll-off past the two pole response of the IC of the converter (see Closing the Feedback Loop).

---

**SOFT-START**

The soft-start function is combined with shutdown. When the SHDN/SS pin is brought above typically 1V, the IC is enabled but the EA duty cycle is clamped from the V_{O} pin. A detailed diagram of this function is shown in Figure 5. The components R_{ES} and C_{PS} provide a slow ramping voltage on the SHDN/SS pin to provide a soft-start function.

**APPLICATION INFORMATION**

**COMPONENT SELECTION**

**Inductor Selection**

The high frequency operation of the LTC3441 allows the use of small surface mount inductors. The inductor current ripple is typically set to 20% to 40% of the maximum inductor current. For a given ripple the inductance terms are given as follows:

\[
L > \frac{V_{MIN} - V_{MAX}}{I_{MAX} - I_{MIN}} \times \frac{100}{\% \text{ Ripple}}
\]

where \(f \) is operating frequency, \(H\), \(\% \text{ Ripple} = \text{allowable inductor current ripple}, \%\), \(V_{MIN} = \text{minimum input voltage}, V\), \(V_{MAX} = \text{maximum input voltage}, V\), \(I_{OUT} = \text{output load current}\).

For high efficiency, choose an inductor with a high frequency core material, such as ferrite, to reduce core losses. The inductor should have low ESR (equivalent series resistance) to reduce the PR losses, and must be able to handle the peak inductor current without saturating. Molded chokes or chip inductors usually do not have enough core to support the peak inductor currents in the 1A to 2A region. To minimize radiation noise, use a toroid, pot core or shielded bobbin inductor. See Table 1 for suggested components and Table 2 for a list of component suppliers.

**Output Capacitor Selection**

The bulk value of the capacitor is set to reduce the ripple due to charge into the capacitor each cycle. The steady state ripple due to charge is given by:

\[
\% \text{ Ripple} = \frac{I_{OUT}(MAX) \times (V_{OUT} - V_{MIN})}{C_{OUT} \times f} \times 100 \%
\]

\[
\% \text{ Ripple} = \frac{I_{OUT}(MAX) \times (V_{MIN} - V_{OUT})}{C_{OUT} \times f} \times 100 \%
\]

where \(C_{OUT} \) is output filter capacitor, \(f\) is operating frequency, \(H\), \(\% \text{ Ripple} = \text{output filter ripple}, \%\), \(V_{MIN} = \text{minimum output voltage}, V\), \(V_{OUT} = \text{maximum output voltage}, V\), \(I_{OUT} = \text{output load current}\).

The output capacitance is usually many times larger in order to handle the transient response of the converter. For a rule of thumb, the ratio of the operating frequency to the unity-gain bandwidth of the converter is the amount the output capacitance will have to increase from the above calculations in order to maintain the desired transient response.

The other component of ripple is due to the ESR (equivalent series resistance) of the output capacitor. Low ESR capacitors should be used to minimize output voltage ripple. For surface mount applications, Taiyo Yuden ceramic capacitors, AXX TPS series tantalum capacitors or Sanyo POSCAP are recommended.
APPLICATIONS INFORMATION

Input Capacitor Selection
Since the $V_{IN}$ pin is the supply voltage for the IC it is recommended to place at least a 4.7μF, low ESR bypass capacitor.

<p>| Table 2. Capacitor Vendor Information |</p>
<table>
<thead>
<tr>
<th>SUPPLIER</th>
<th>PHONE</th>
<th>FAX</th>
<th>WEB SITE</th>
</tr>
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<tbody>
<tr>
<td>AVX</td>
<td>(030) 448-9411</td>
<td>(030) 448-9434</td>
<td><a href="http://www.avxcorp.com">www.avxcorp.com</a></td>
</tr>
<tr>
<td>Sonyo</td>
<td>(619) 661-3222</td>
<td>(619) 661-1066</td>
<td><a href="http://www.sanyovideo.com">www.sanyovideo.com</a></td>
</tr>
<tr>
<td>Taiyo Yuden</td>
<td>(003) 571-550</td>
<td>(003) 571-4159</td>
<td><a href="http://www.t-yuden.com">www.t-yuden.com</a></td>
</tr>
</tbody>
</table>

Optional Schottky Diodes
The Schottky diodes are used across the synchronous switches B and D are not required ($V_{OUT} < 4.3V$), but allow lower efficiency of the NMOS to PMOS transition. Improving efficiency, Schottky diode such as an MBRM1203 is acceptable. Do not use ordinary rectifier diodes, since the slow recovery times will compromise efficiency. For applications with an output voltage above 4.3V, a Schottky diode is required from SW2 to VOUT.

Output Voltage < 2.4V
The LTC3441 can operate as a buck converter with output voltages as low as 3.4V. The part is specified at 2.4V minimum to allow operation without the requirement of a Schottky diode. Synchronous switch D is powered from VOUT and the $R_{SW}$ will increase at low output voltages, therefore a Schottky diode is required from SW2 to VOUT to provide the current path to the output.

Output Voltage > 4.3V
A Schottky diode from SW1 to VOUT is required for output voltages over 4.3V. The diode must be located as close to the pins as possible in order to reduce the peak voltage on SW2 due to the parasitic gate and trace inductance.

Input Voltage > 4.5V
For applications with input voltages above 4.5V which could exhibit an overload or short-circuit condition, a $2x/2\mu F$ series snubber is required between the SW1 pin and GND. A Schottky diode from SW1 to VOUT should also be added as close to the pins as possible. For the higher

---

![Figure 7. Error Amplifier with Type I Compensation](image1)

The unity-gain frequency of the error amplifier with the Type I compensation is given by:

$$f_{UG} = \frac{1}{2\pi R_1 C_{P1}} \text{Hz}$$

Most applications demand an improved transient response to allow a smaller output filter capacitor. To achieve a higher bandwidth, Type III compensation is required. Two zeros are required to compensate the double-pole response.

$$f_{POLE1} = \frac{1}{2\pi R_C C_{P1}} \text{Hz}$$
$$f_{ZERO1} = \frac{1}{2\pi R_2 C_{P1}} \text{Hz}$$
$$f_{ZERO2} = \frac{1}{2\pi R_3 C_{P2}} \text{Hz}$$

Which is extremely close to DC

$1 \text{Hz}$

The component values of Type III compensation is given by:

$$f_{POLE2} = \frac{1}{2\pi R_C C_{P2}} \text{Hz}$$

The loop gain is typically rolled off before the RHP zero frequency.

A simple Type I compensation network can be incorporated to stabilize the loop at a cost of reduced bandwidth and slower transient response. To ensure proper phase margin, the loop requires to be crossed over in a decade before the LC double pole.

---

![Figure 8. Error Amplifier with Type III Compensation](image2)

---

![Figure 9. Fast Transient Response Compensation for Step Load or Mode Change](image3)
Features
- Carrier Frequency f<sub>peak</sub> 100 kHz - 150 kHz
- Typical Data Rate up to 5 kbaud at 125 kHz
- Suitable for Manchester and Bi-phase Modulation
- Power Supply from the Car Battery or from 5-V Regulated Voltage
- Optimized for Car Immobilizer Applications
- Tuning Capability
- Microcontroller-compatible Interface
- Low Power Consumption in Standby Mode
- Power-supply Output for Microcontroller

Applications
- Car Immobilizers
- Animal Identification
- Access Control
- Process Control

Description
The U2270B is an IC for ID/IC<sup>®</sup> read/write base stations in contactless identification and immobilizer systems. The IC incorporates the energy-transfer circuit to supply the transponder. It consists of an on-chip power supply, an oscillator and a coil driver optimized for automotive-specific distances. It also includes all signal-processing circuits which are necessary to transform the small input signal into a microcontroller-compatible signal.

System Block Diagram

![System Block Diagram](image-url)

**Pin Configuration**

**Figure 1. Pinning**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
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</tr>
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<td>MS</td>
<td>Mod select coil 1: common mode/differential mode</td>
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<td>6</td>
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<td>VBAT</td>
<td>Battery voltage</td>
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<td>14</td>
<td>VS</td>
<td>Internal power supply (5 V)</td>
</tr>
<tr>
<td>15</td>
<td>RF</td>
<td>Frequency adjustment</td>
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<td>16</td>
<td>HIFASS</td>
<td>DC decoupling</td>
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